Verification of Concurrent Programs under Relaxed Memory Models

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Concurrent Programs with Shared Memory

- Finite number of shared variables $\{x, y, x_1, \ldots\}$
- Finite data domain $\{d, d_0, d_1, \ldots\}$
- Finite number of finite-control threads $T_1, \ldots, T_n$ with operations:

$$w(x, d), \quad r(x, d)$$

$x = y = 0$

Thread 1	Thread 2
$a: x = 1$	$p: y = 1$
$b: if(y == 0)\{$	$q: if(x == 0)\{$
$c: \quad crit.sect.1$	$r: \quad crit.sect.2$
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Dekker's mutual exclusion protocol.

Sequential Consistency (SC) Semantics [Lamport 1979]

- Threads directly write to and read from memory
- Classical interleaving semantics
  - Computations of different threads are shuffled
  - Program order is preserved for each thread

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	Mem
Thread 1	x
$pc = a$	0
Thread 2	y
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Thread 1
$pc = b$

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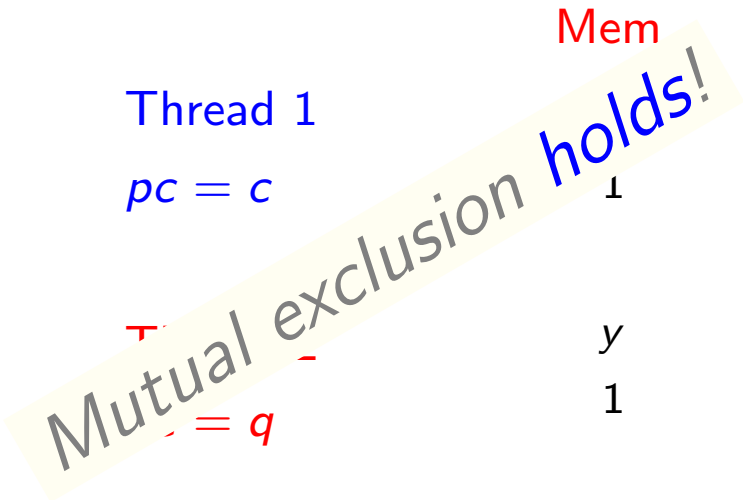

Total Store Ordering (TSO) Semantics [SPARC 1994, x86]

- Sequential Consistency forbids compiler and hardware optimizations
- Hence is not implemented by any processor
- Processors have various buffers to reduce latency of memory accesses
- Behavior captured by relaxed memory models
- Here: Total Store Ordering (TSO) memory model

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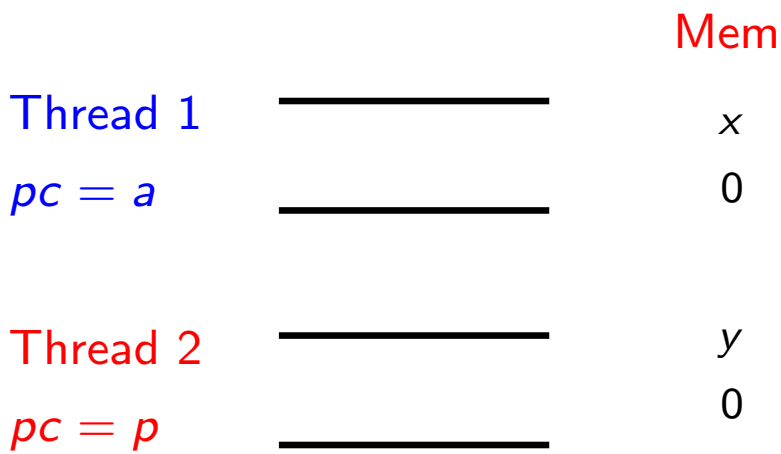

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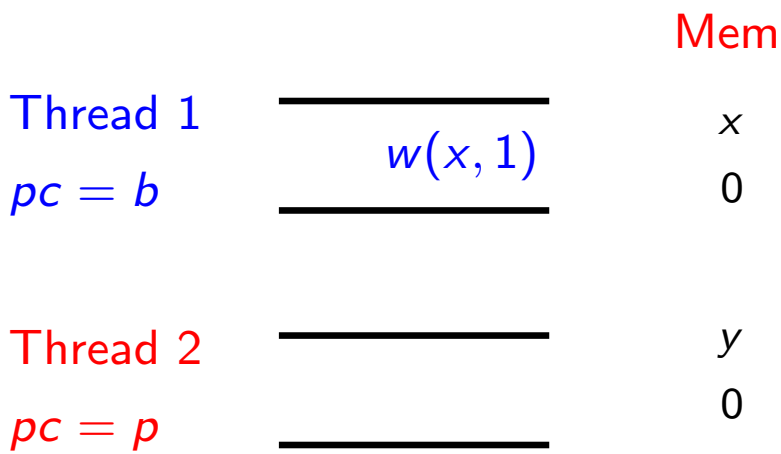

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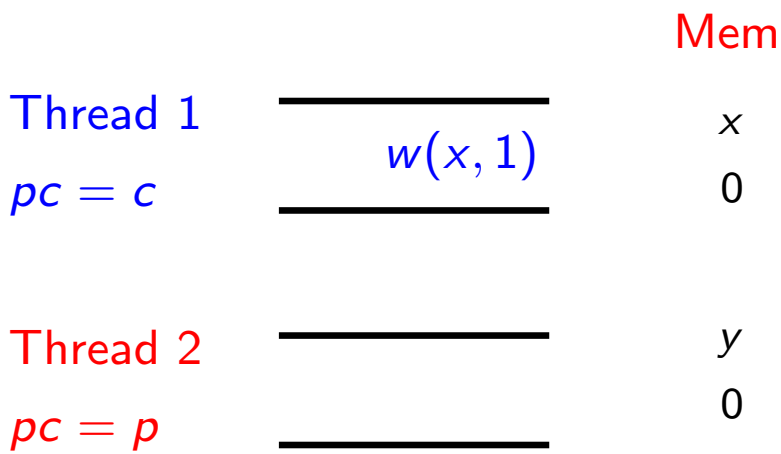

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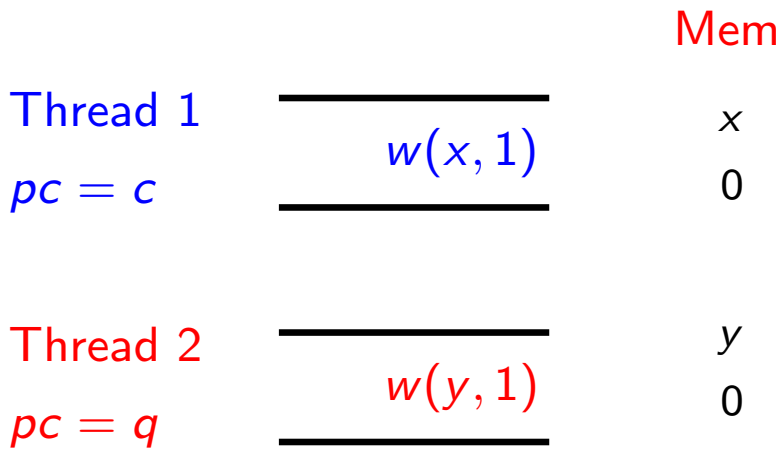

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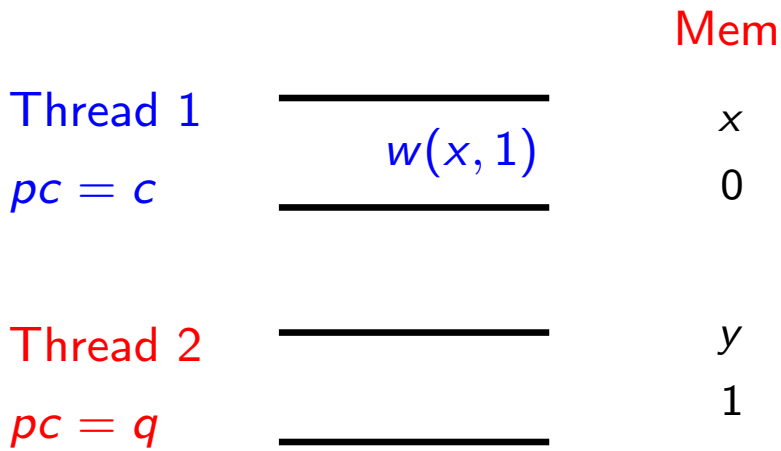

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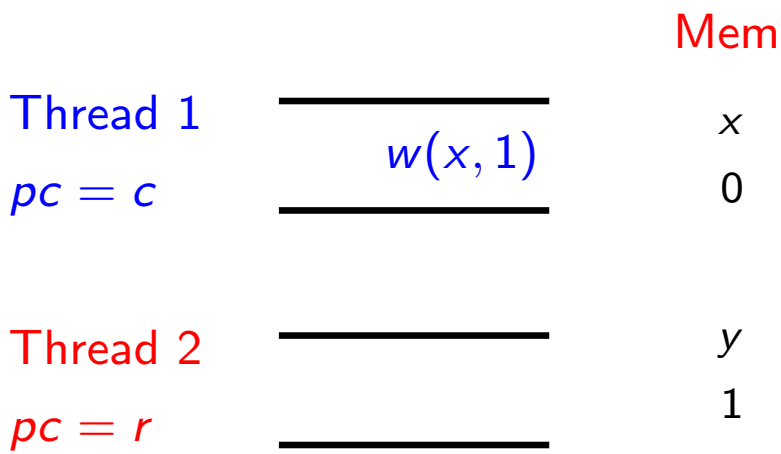

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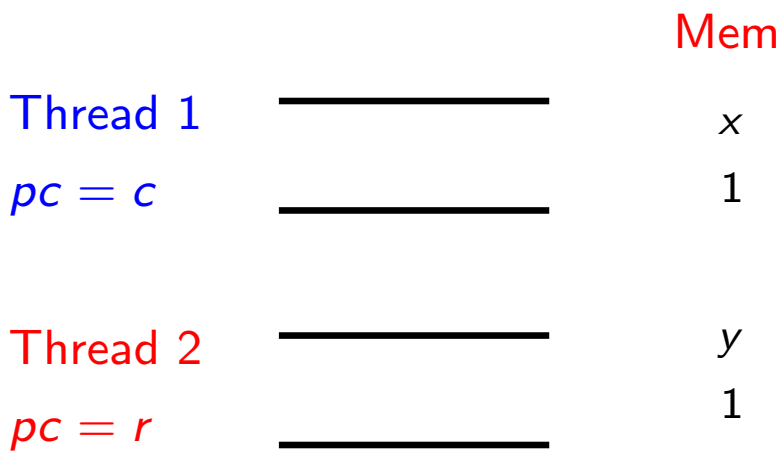

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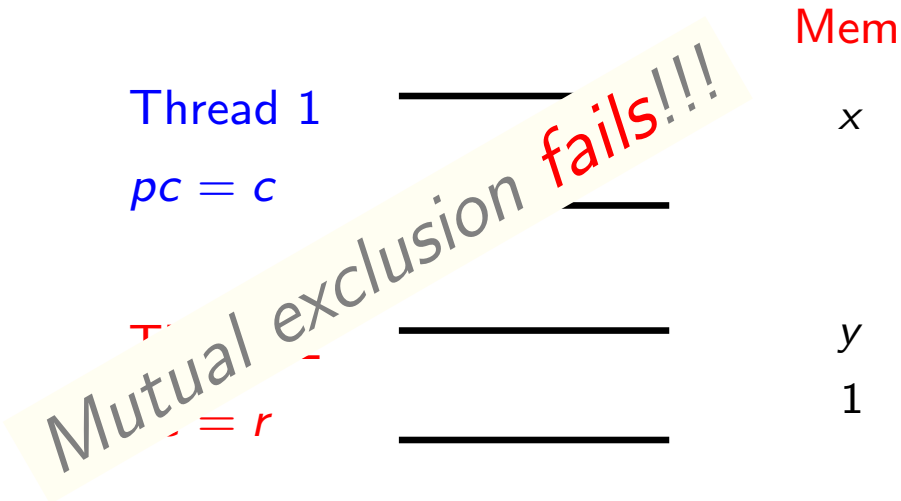

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This is where our verification techniques apply

Outline

Reachability

[Atig, Bouajjani, Burckhardt, Musuvathi, POPL'10]

State Reachability Problem

Consider a memory model *MM*

State Reachability Problem for *MM*

Input: *Program P and a (control + memory) state s.*

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Each thread is finite-state

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- For the SC memory model, this problem is PSPACE-complete
- Non-trivial for relaxed memory models:

$$Paths_{TSO}(P) = Closure_{TSO}(Paths_{SC}(P)) \text{ is non-regular}$$

Reachability

[Atig, Bouajjani, Burckhardt, Musuvathi, POPL'10]

Decidability:

Simulation of TSO semantics by Lossy Channel Systems

Decidability of State Reachability for TSO

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Corollary

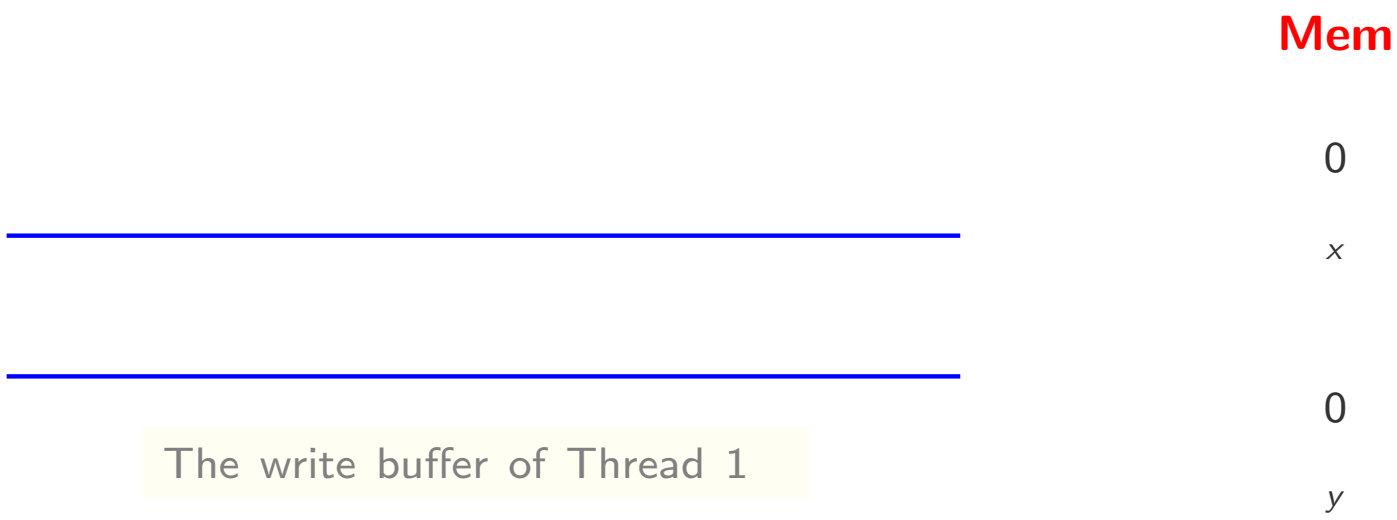
The state reachability problem for TSO is decidable.

From TSO to LCS 1/5

Thread 1: $x = 1;\ y = 1;\ x = 2;\ y = 2;\ y = 3;$

Thread 2: $\text{if } (x == 2)\ \{\quad \text{if } (y == 0)\ \{\ldots\}\quad \}$

Write buffers are perfect FIFO channels



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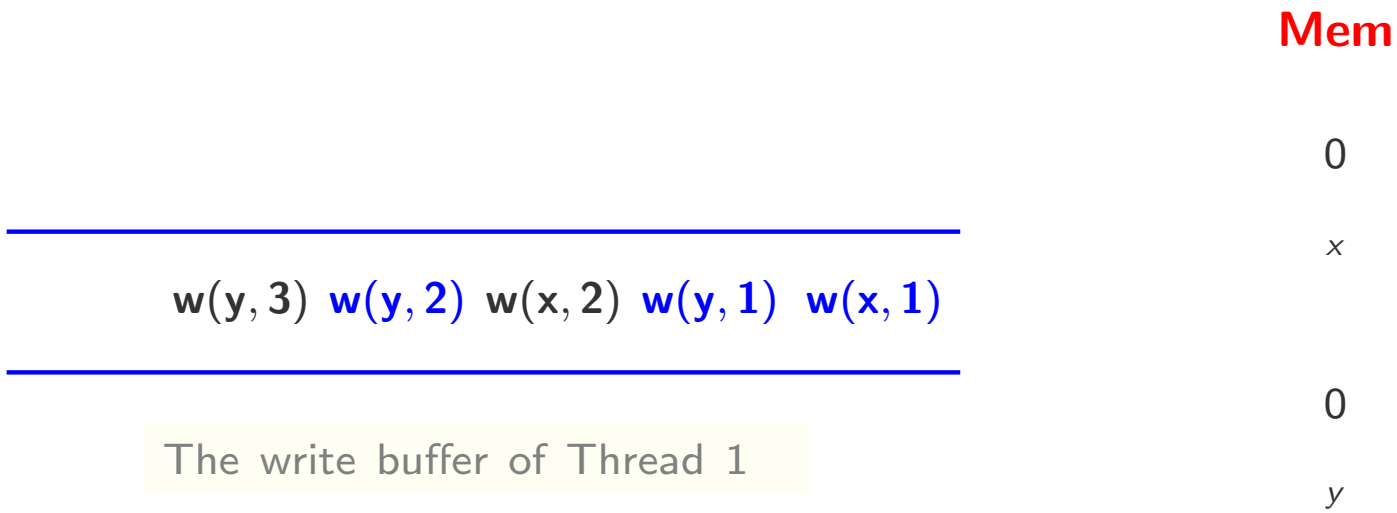

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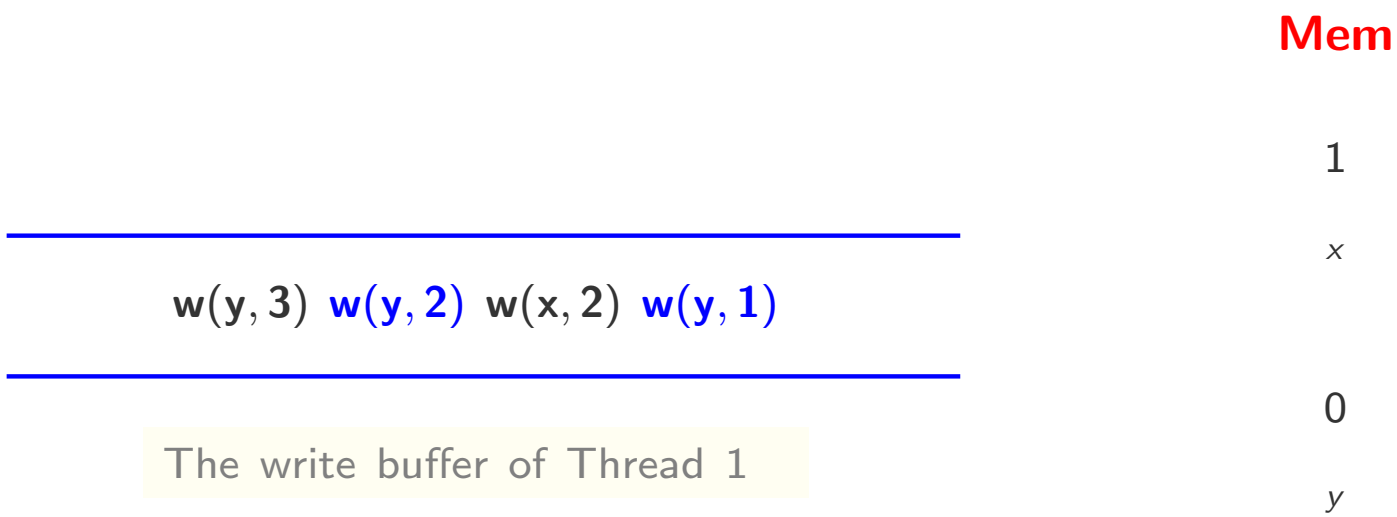

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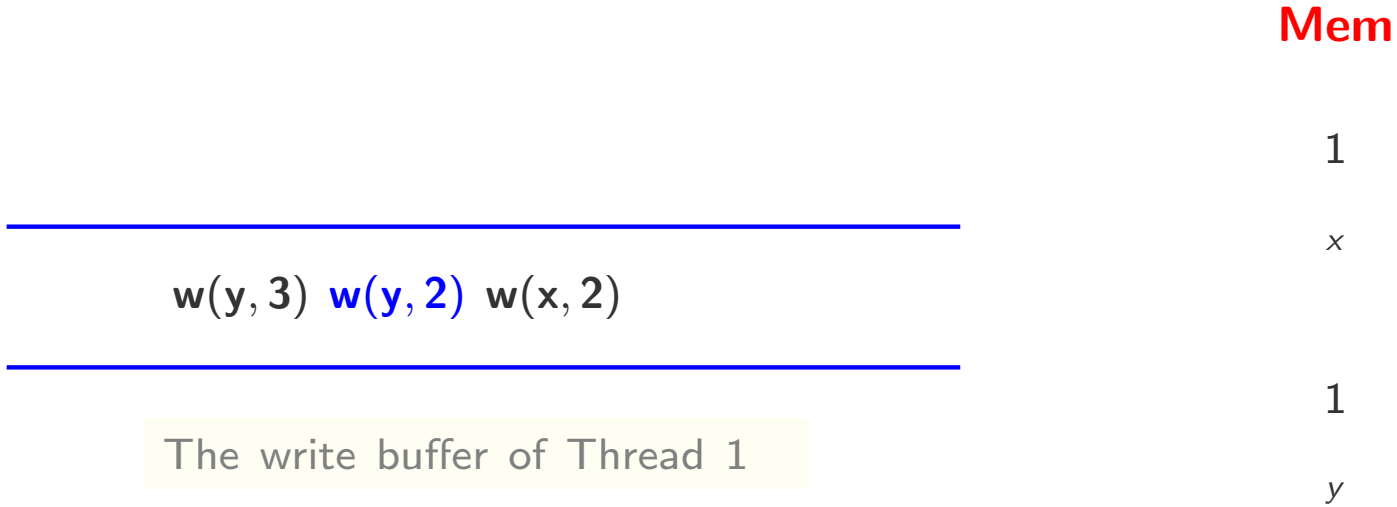

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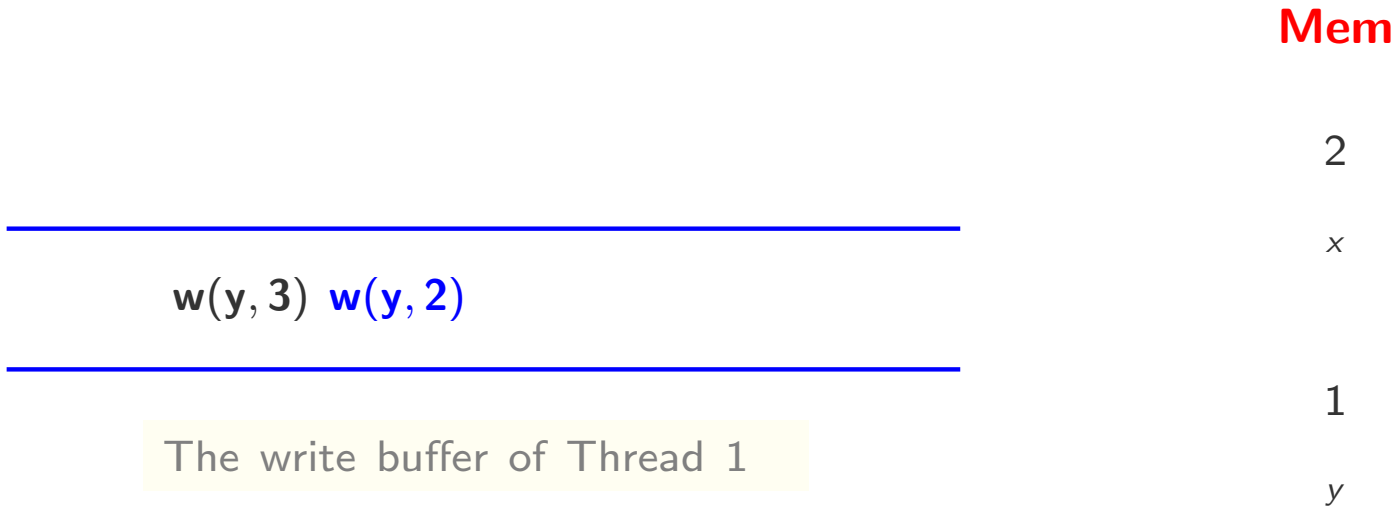

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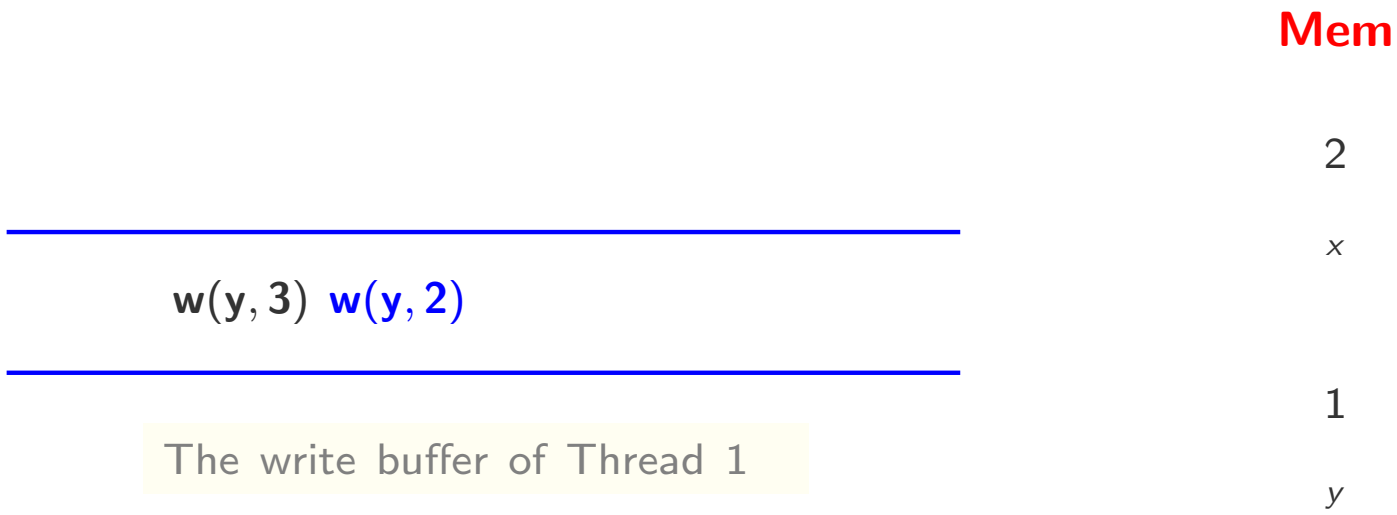

Thread 2 reads x = 2

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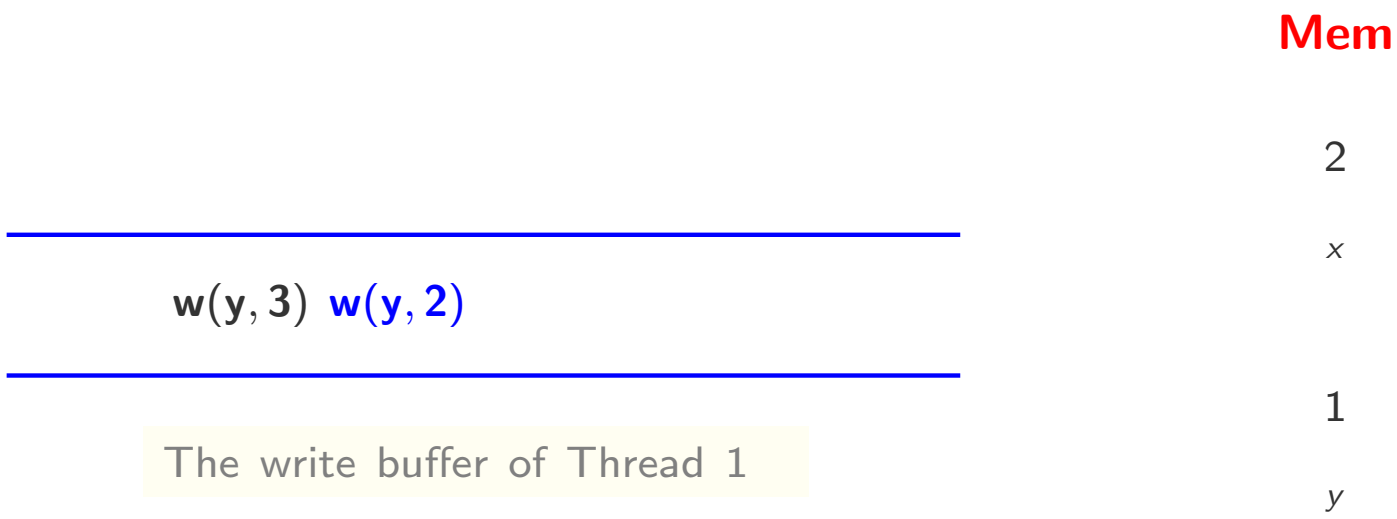

Thread 2 deadlocks as y = 1

From TSO to LCS 2/5

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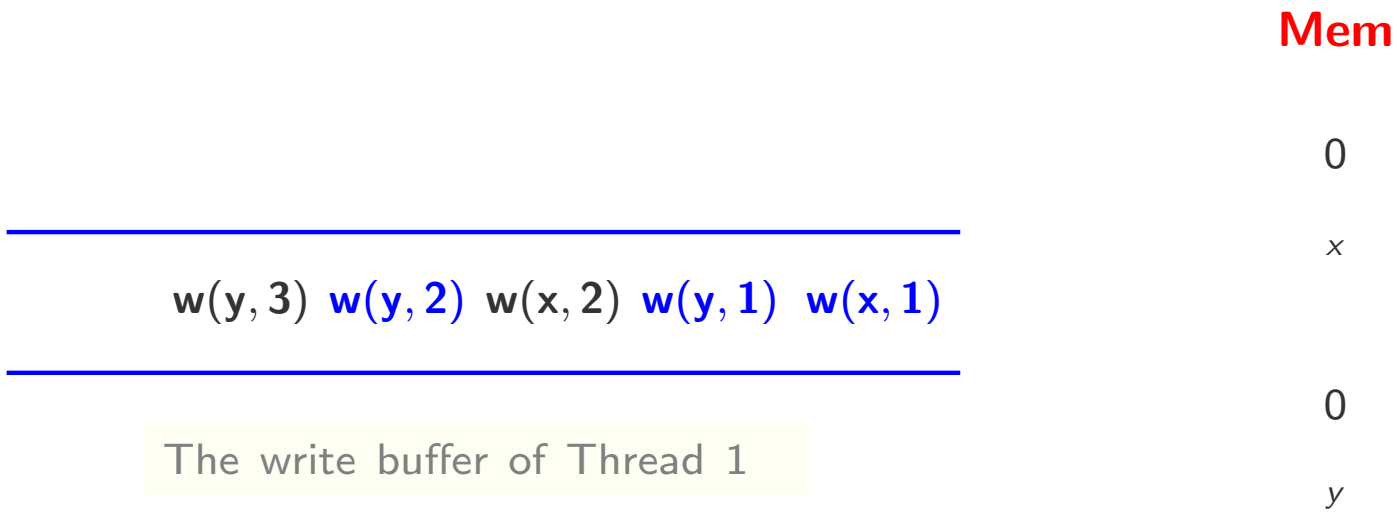
- Batch processing is similar to lossiness
- So assume write buffers are lossy FIFO channels



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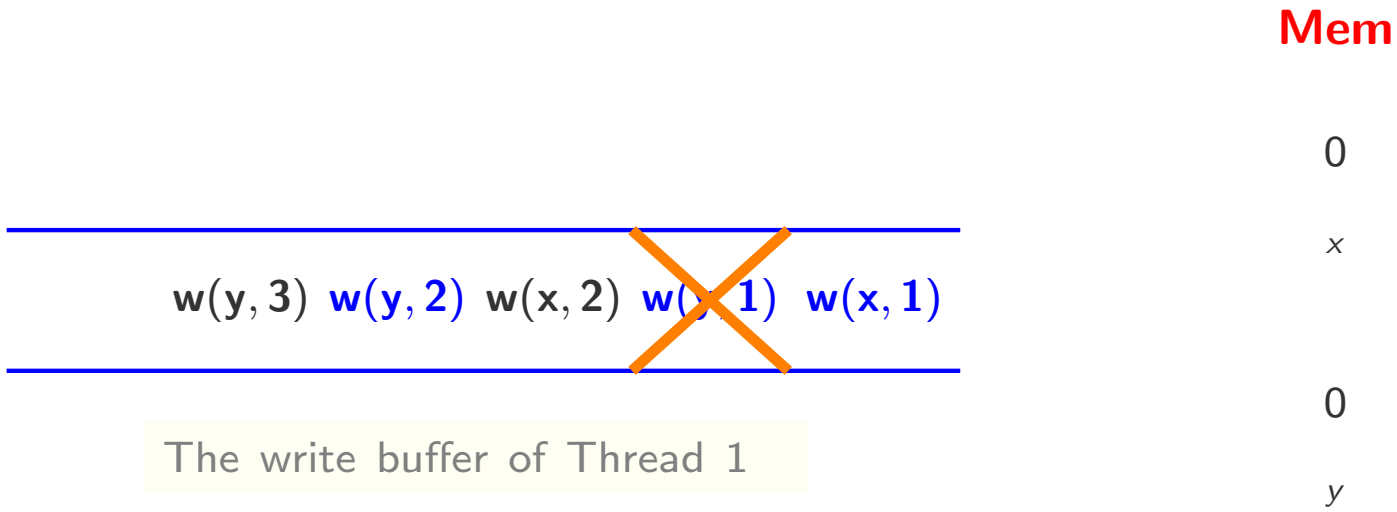

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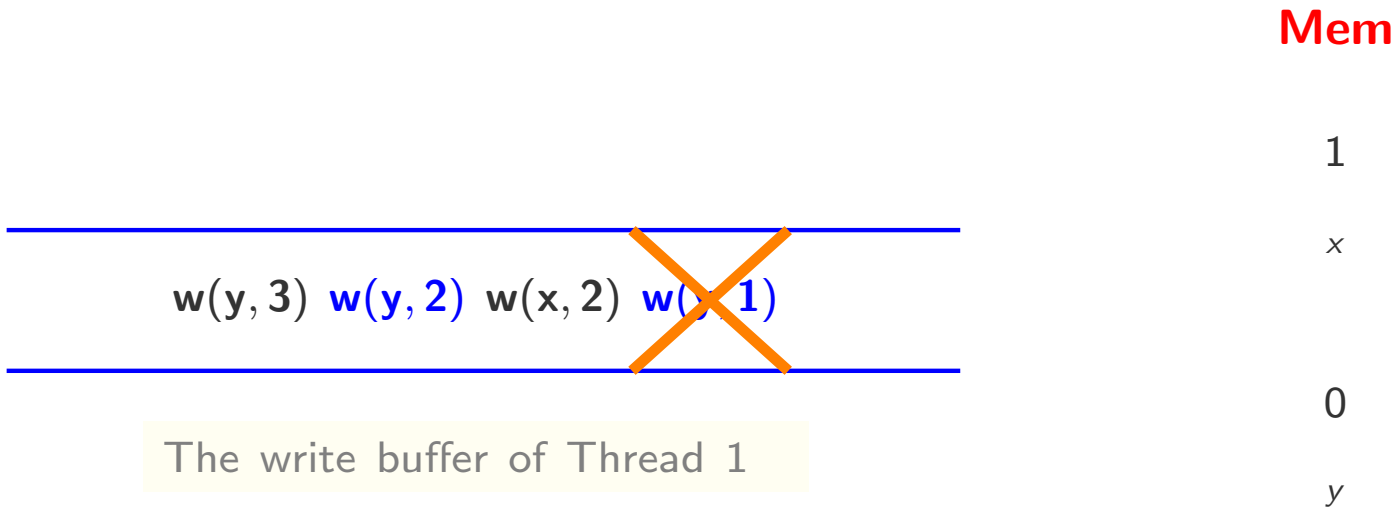

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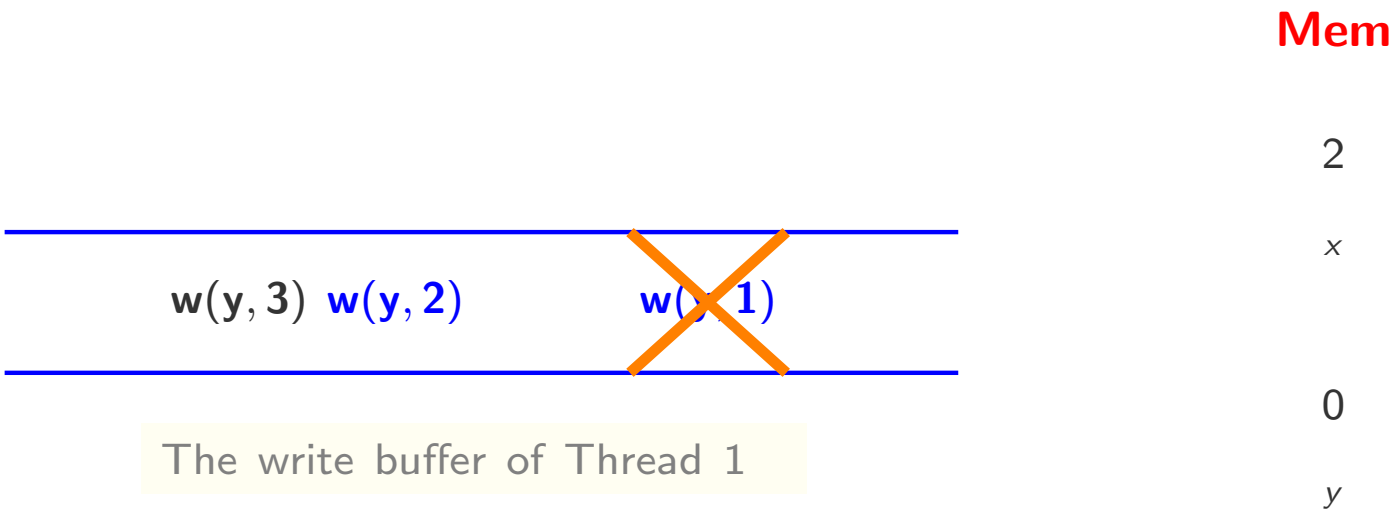

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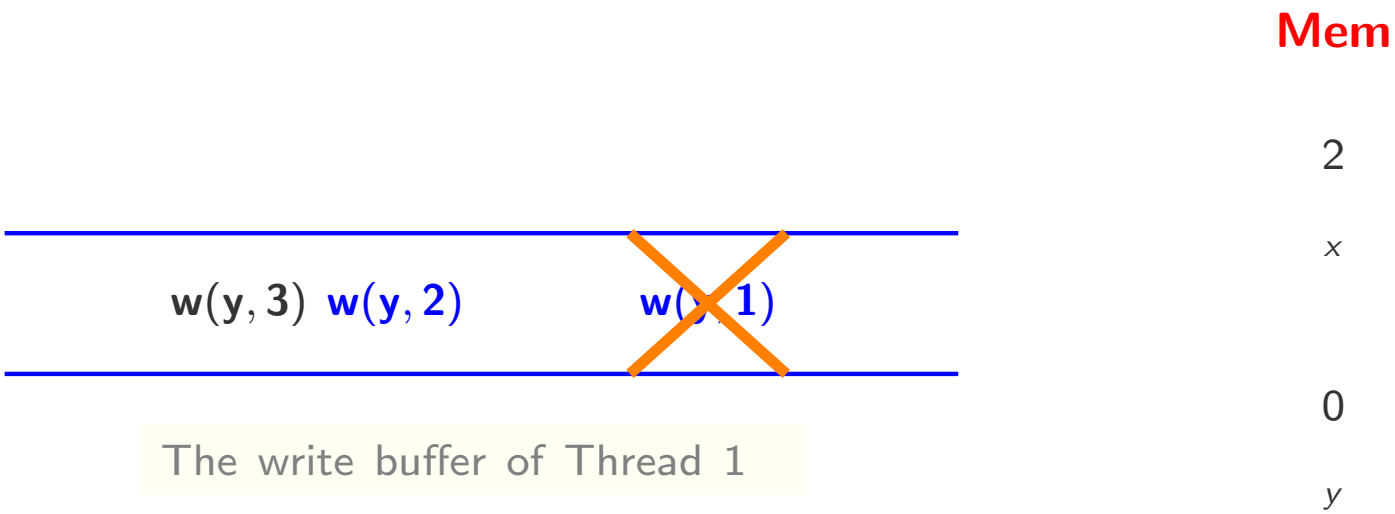

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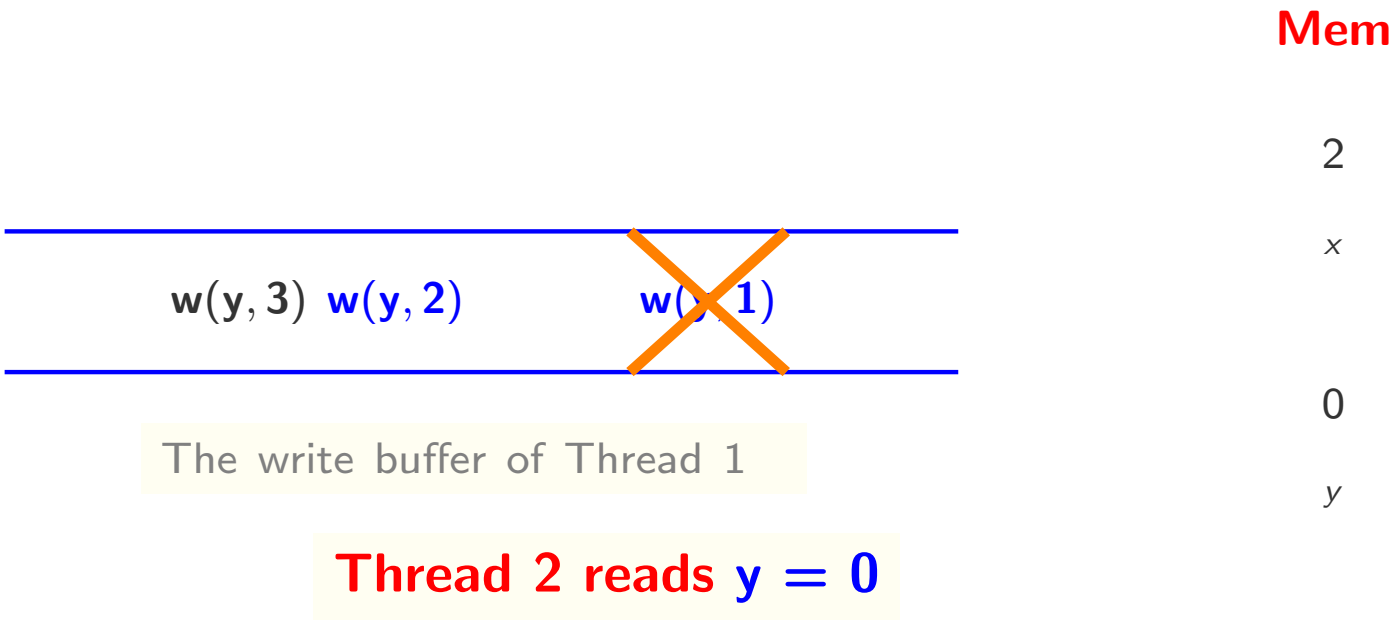

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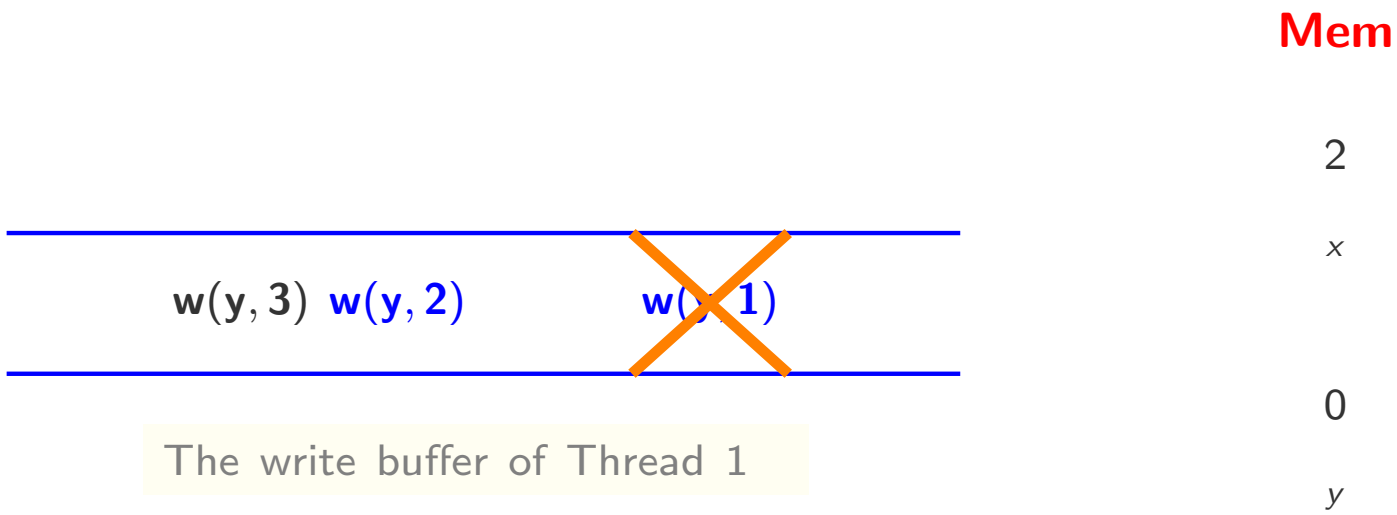
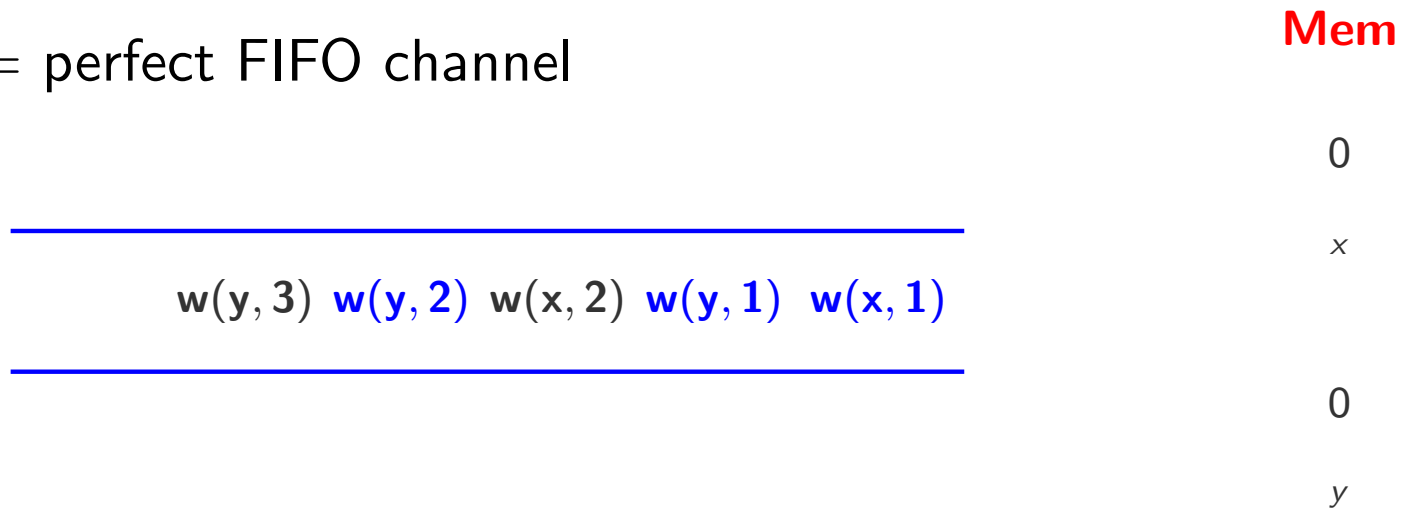


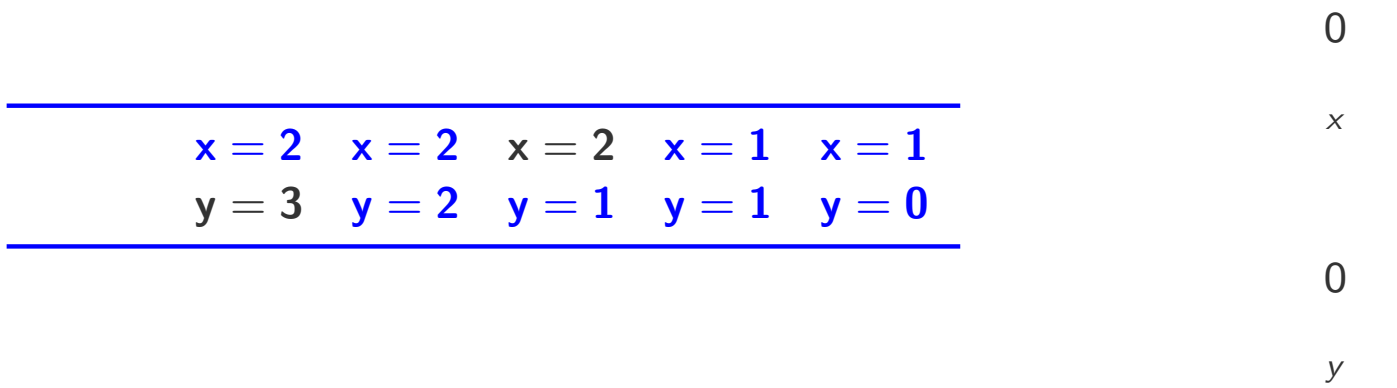
This is wrong! Lost the effect of w(y, 1).

From TSO to LCS 3/5

TSO buffer = perfect FIFO channel

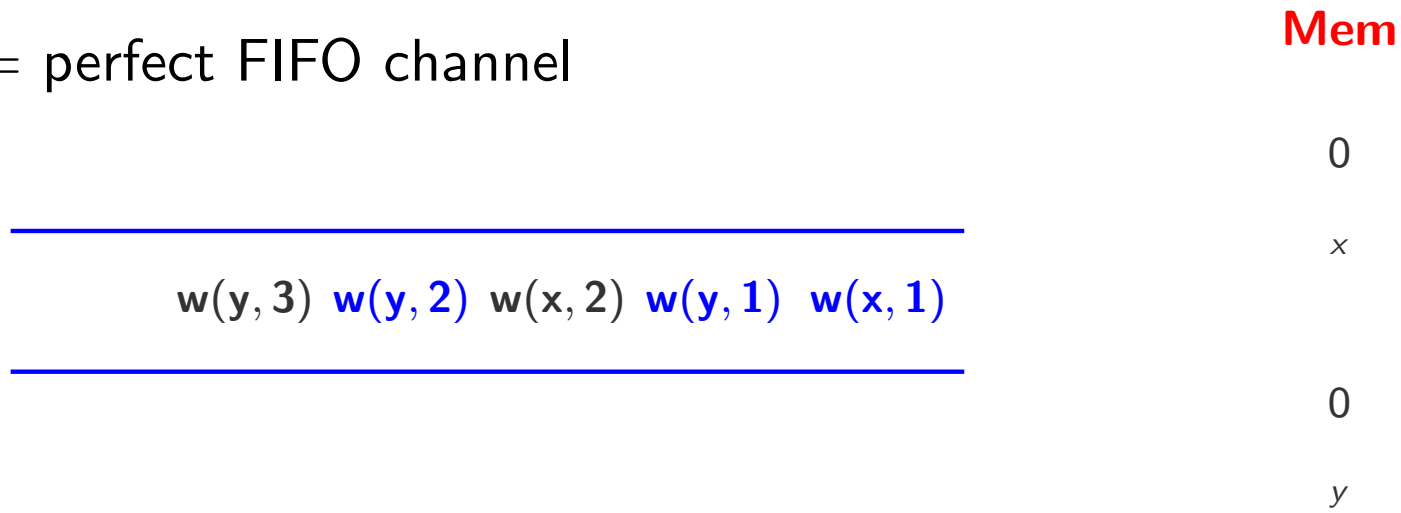


Channel = sequence of memory states + lossiness



From TSO to LCS 3/5

TSO buffer = perfect FIFO channel



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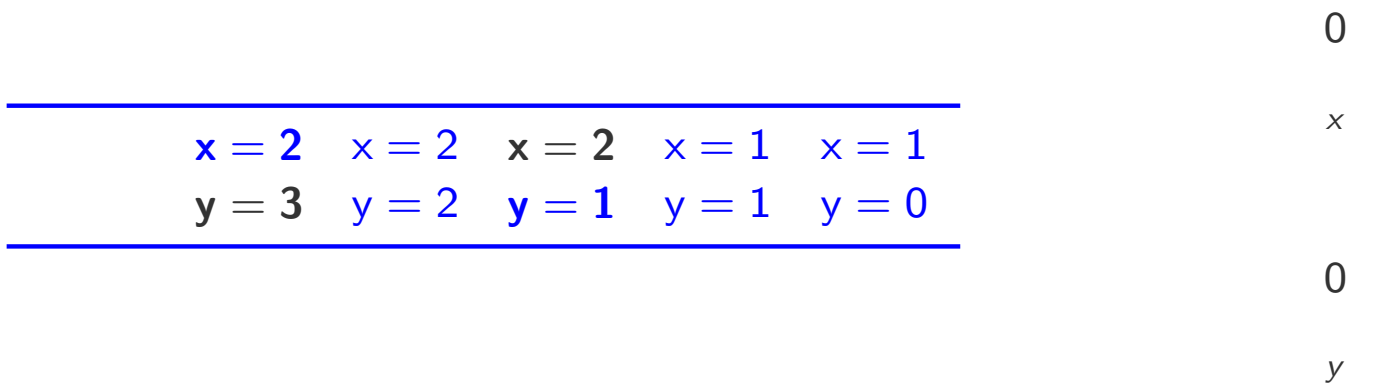

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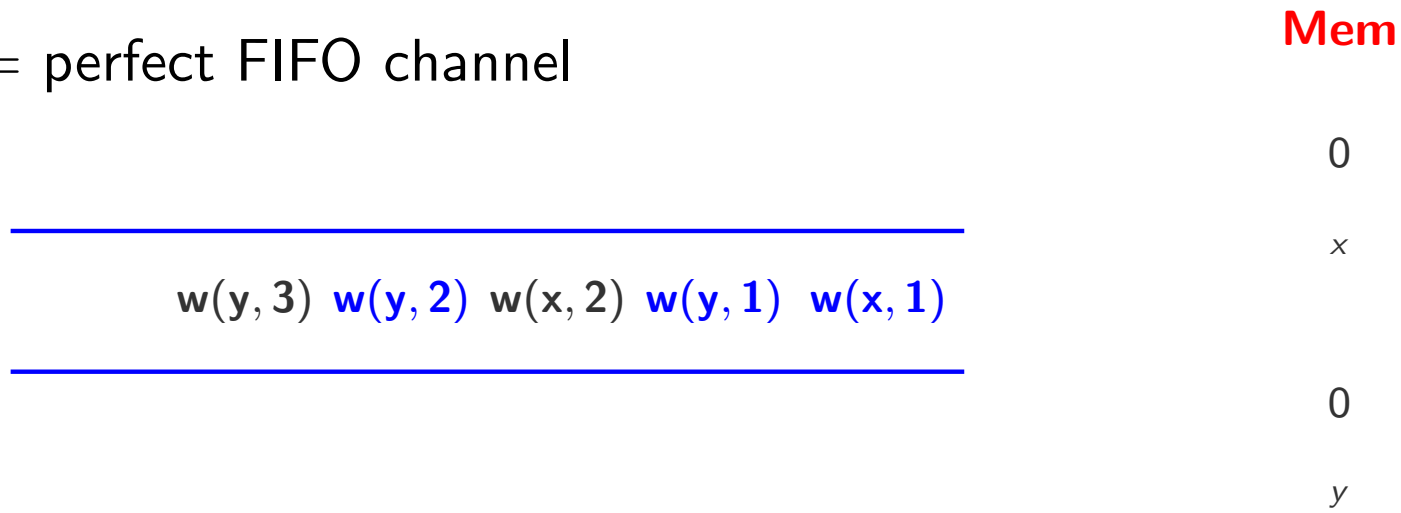

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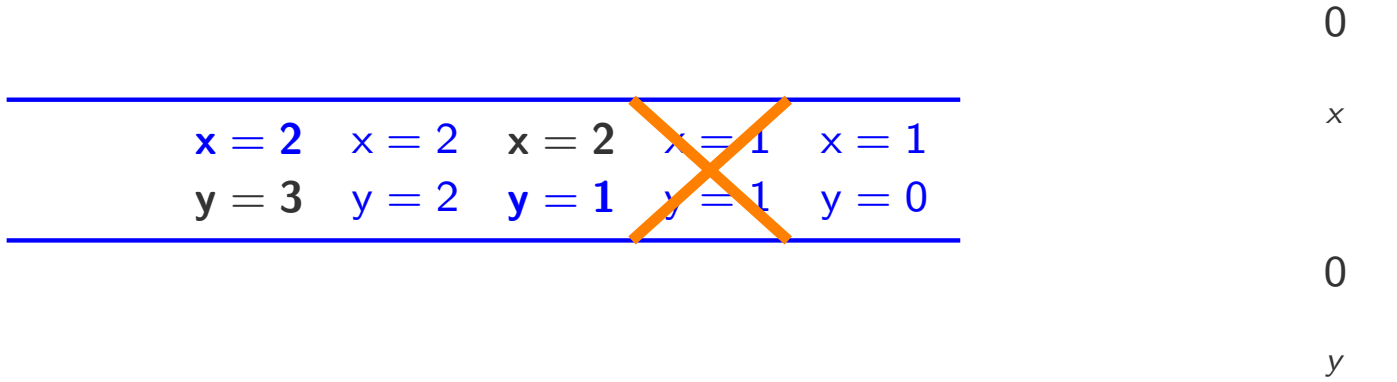

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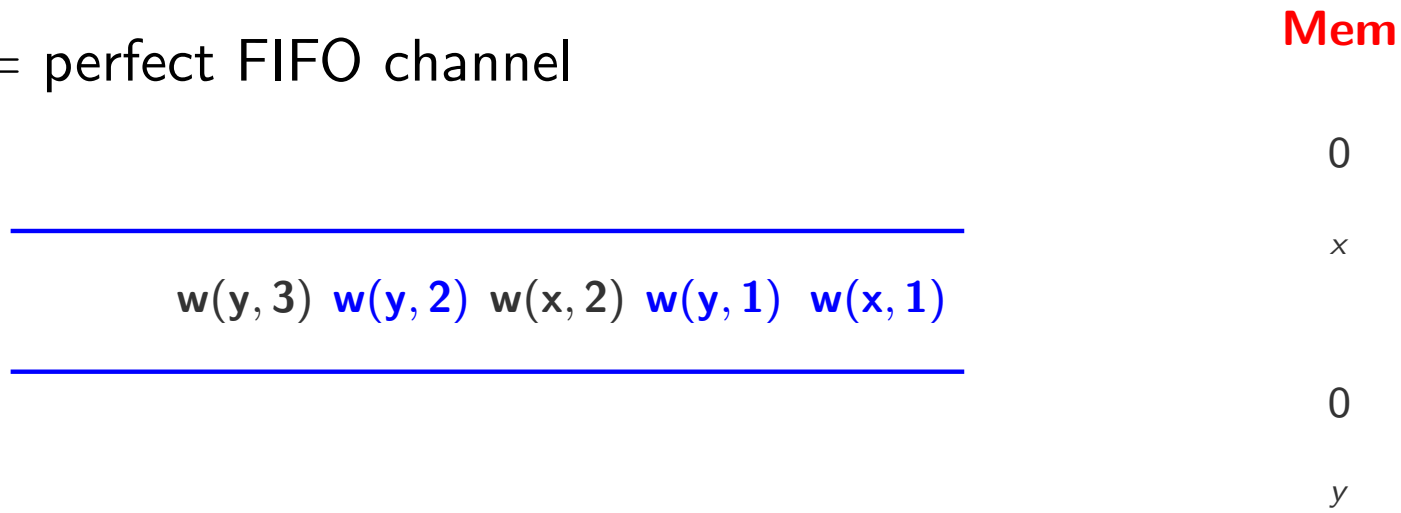

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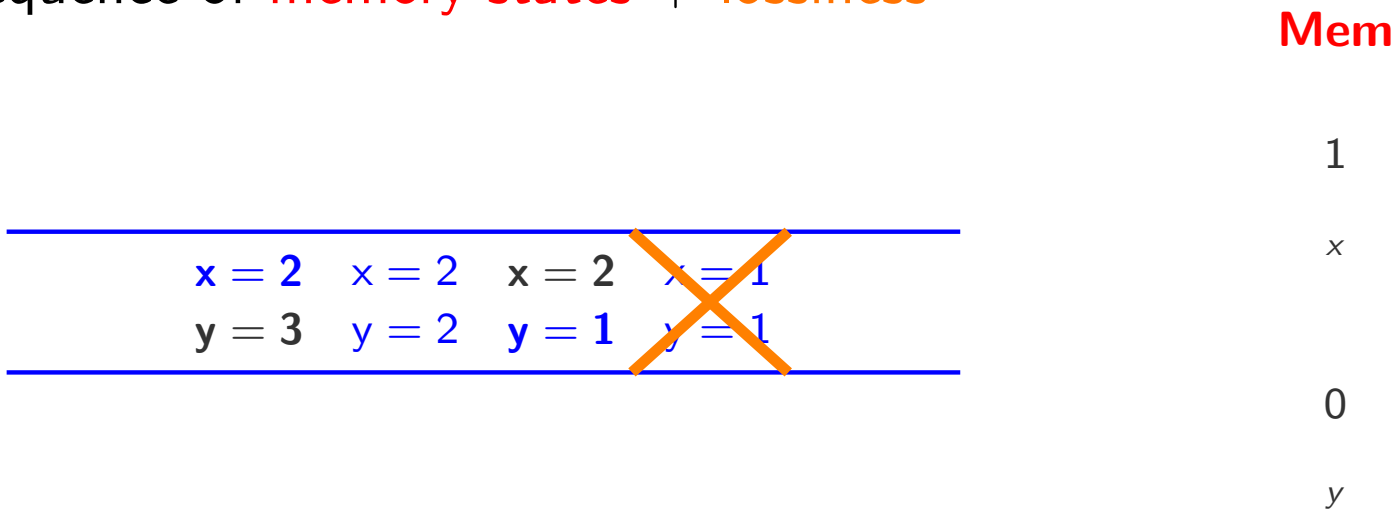

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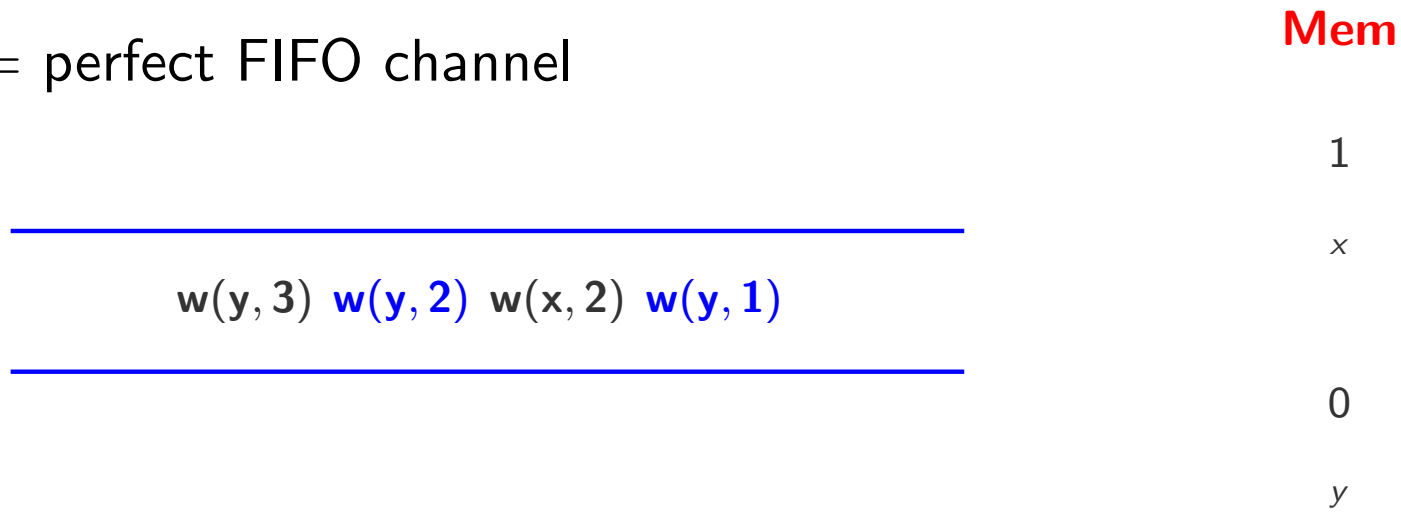

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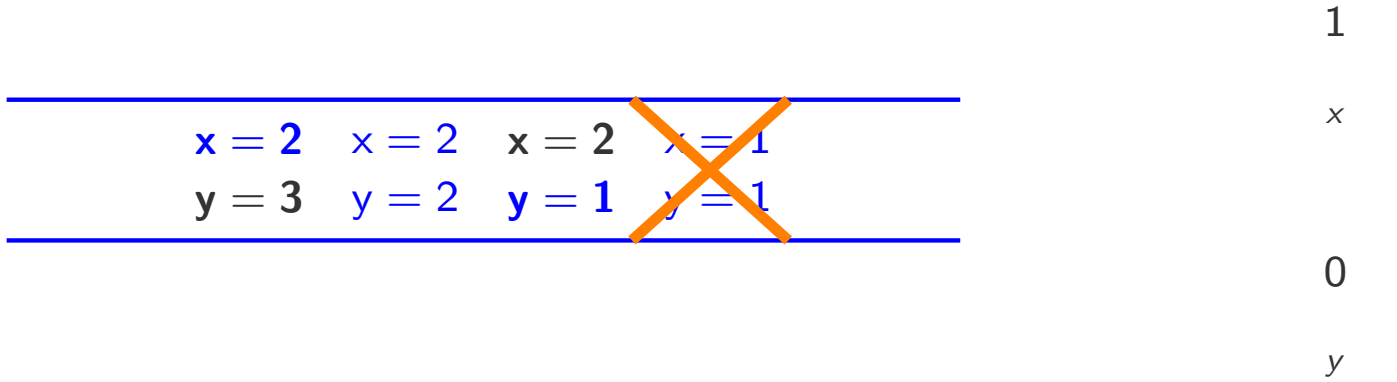

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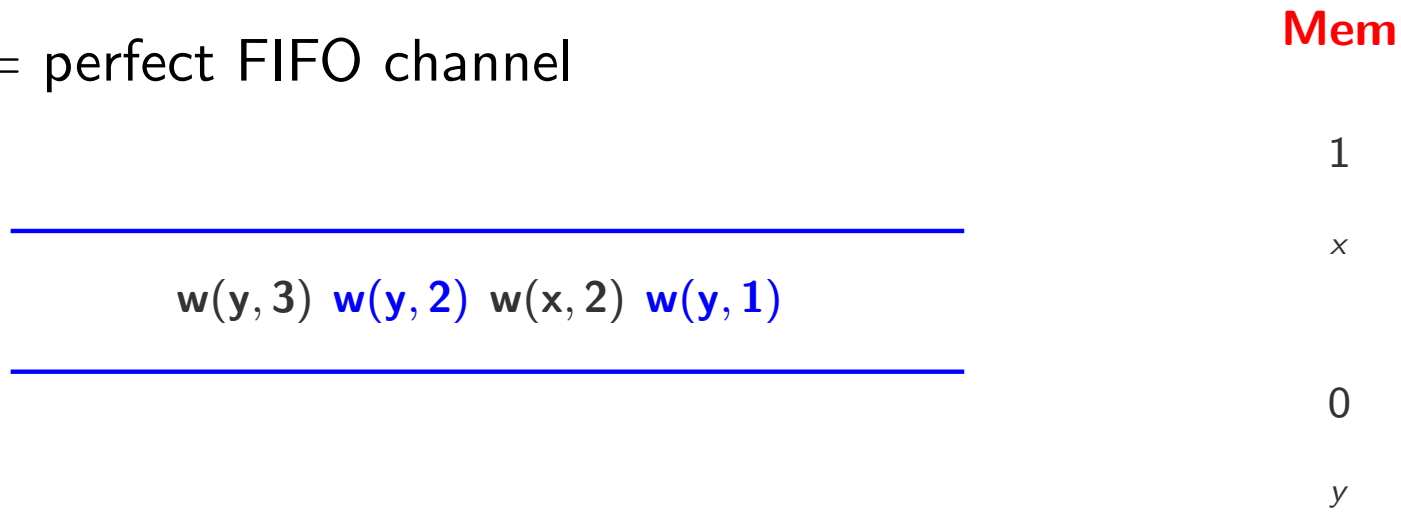

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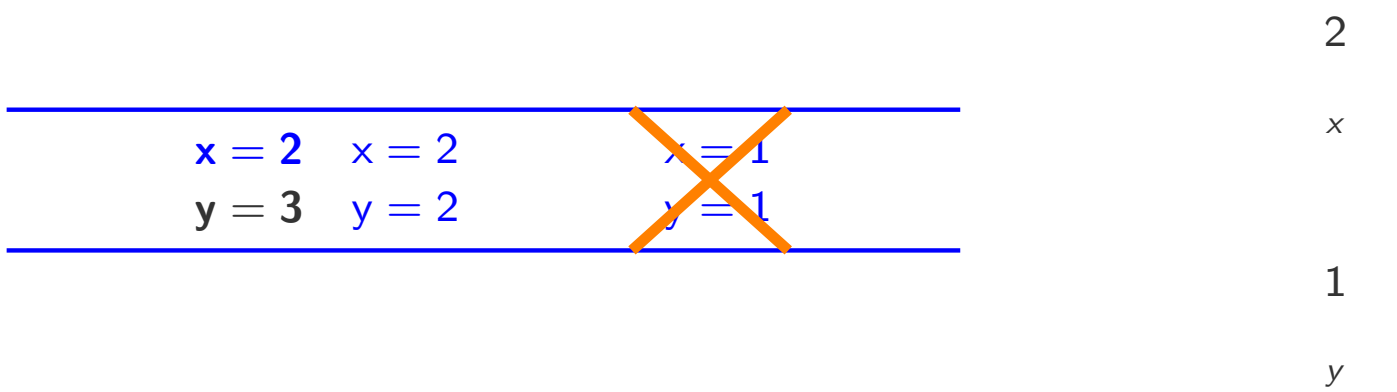

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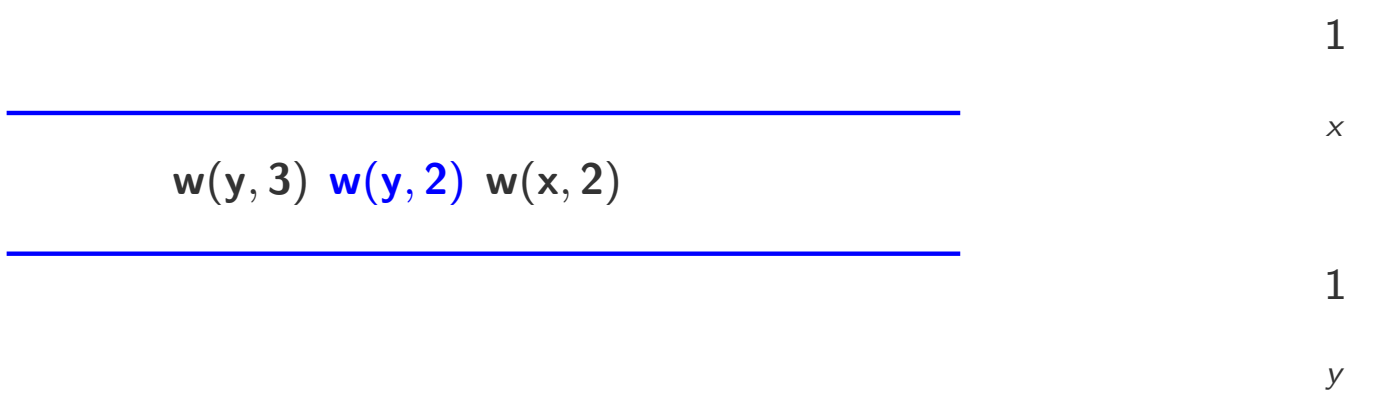

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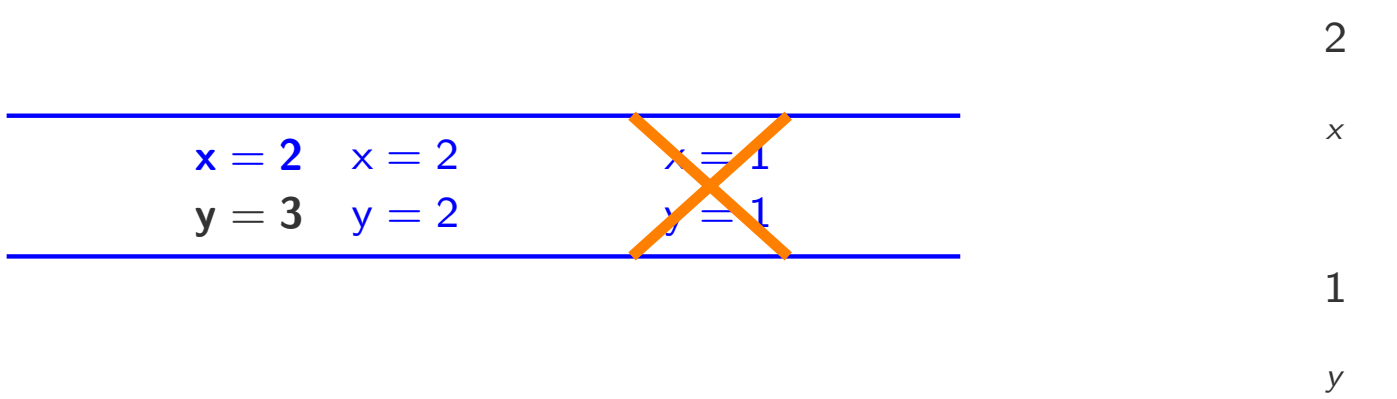

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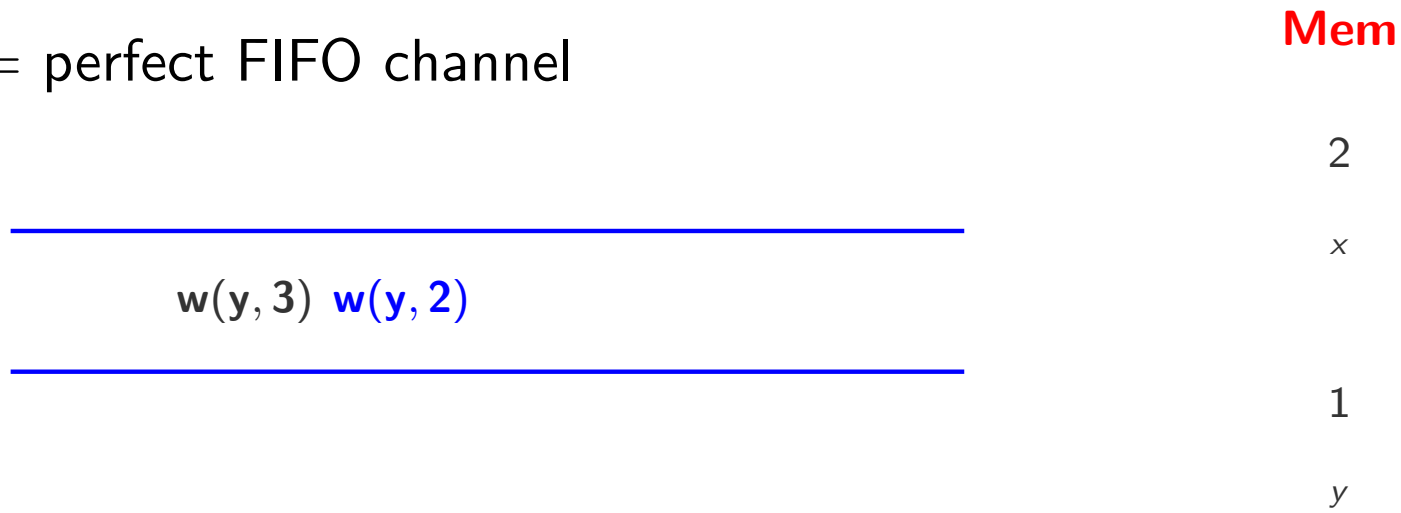

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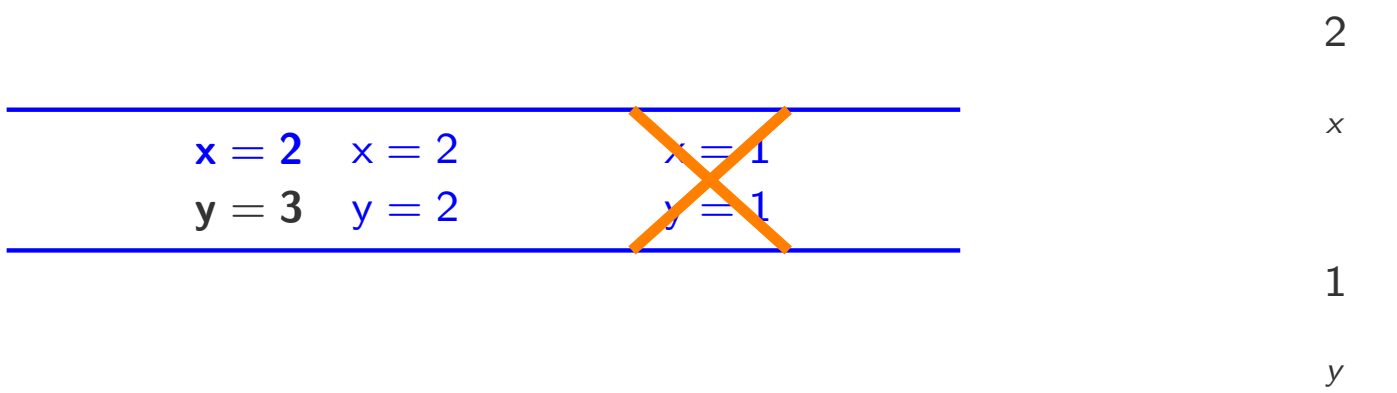

Lossiness = unobservable memory states

From TSO to LCS 4/5

- *Write:* *Compute a new memory state; send it to the channel*
- *Read:* *Check the channel/memory*
- *Memory update:* *Receive a state; copy it to the memory*

From TSO to LCS 4/5

Problem: Interference between threads?

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From TSO to LCS 4/5

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Each thread guesses writes of other threads

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Synchronization of the LCS over send actions

From TSO to LCS 5/5

Theorem [ABBM 2010]

The state reachability problem for TSO is reducible to the control-state reachability problem for LCS.

State Reachability: Conclusion

- Decidable for TSO (and beyond)
- But it is a hard problem — non-primitive recursive
- However, it is possible to have efficient analysis techniques
- Abstraction-based techniques:

  e.g., [Kuperstein, Vechev, Yahav, PLDI'11]

- Symbolic techniques:

  [Abdulla, Atig, Chen, Leonardson, Rezine, TACAS'12]
  [Linden, Wolper, SPIN'10'11]

Robustness

[Bouajjani, M., Möhlmann, ICALP'11]

[Bouajjani, Derevenetc, M., ESOP'13]

Robustness against TSO

Idea of robustness:

TSO behavior that deviates from SC is a programming error

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Trace Robustness:

TSO- and SC-traces are the same [Shasha, Snir'88]

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TSO- and SC-traces are the same [Shasha, Snir'88]

Good: Allows for quite relaxed behaviors

Very Good: Only PSPACE-complete

Traces 1/2

Computation = sequence of actions as seen by memory

$x = y = 0$

Thread 1	Thread 2
$a : x = 1$	$p : y = 1$
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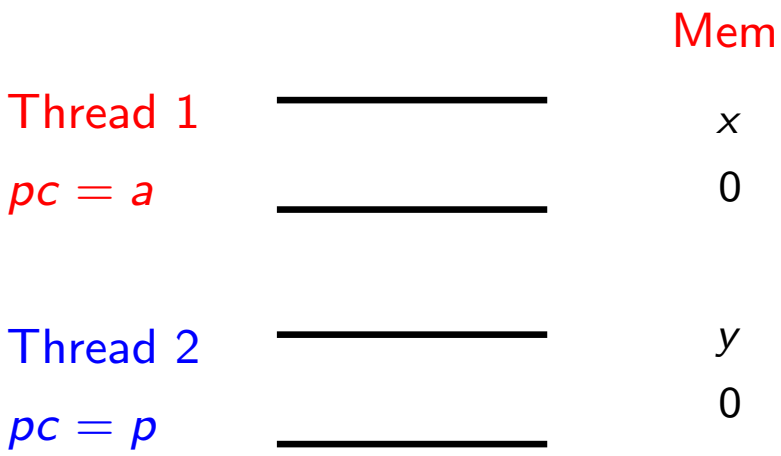

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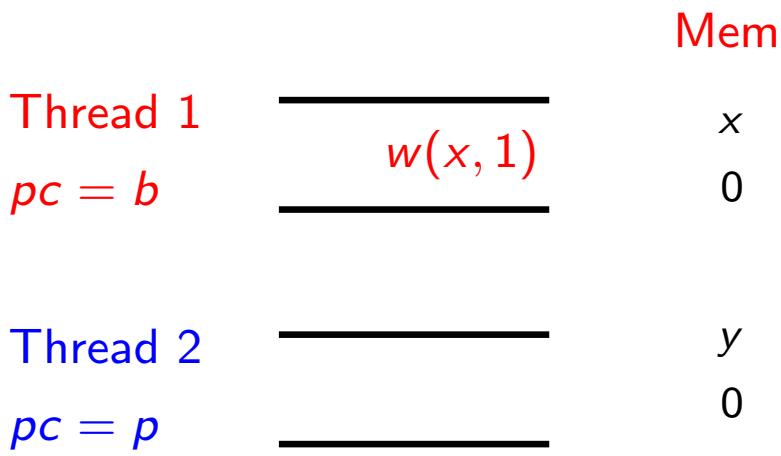

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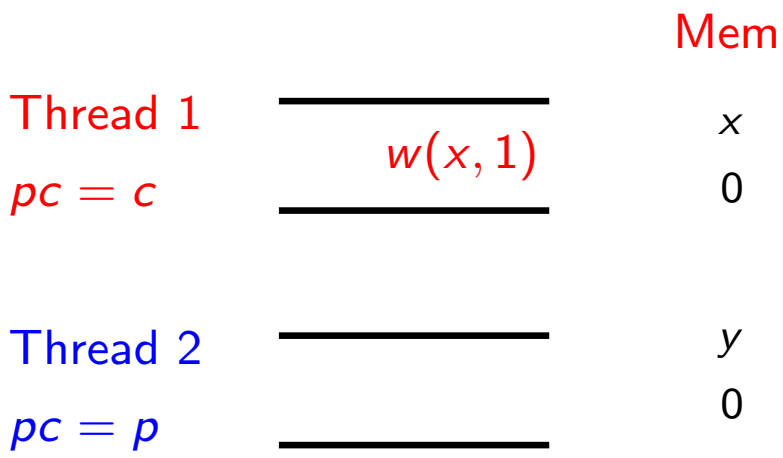

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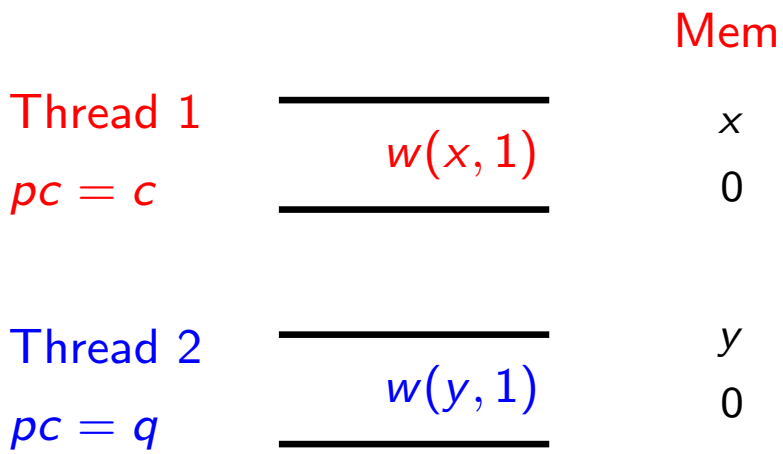

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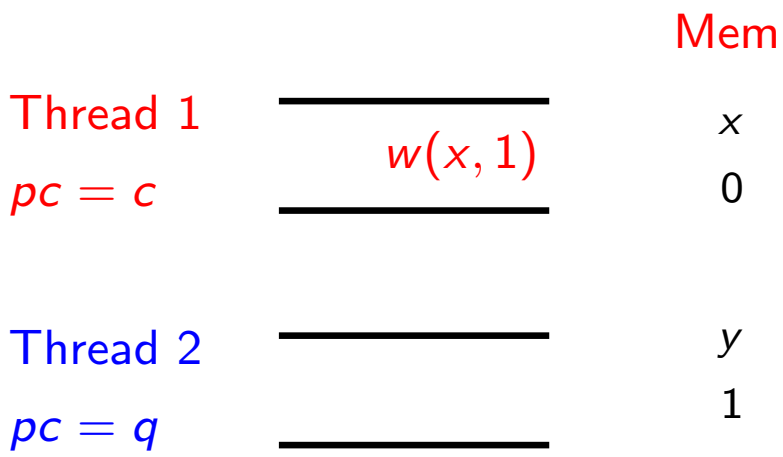

$r(y, 0) \cdot w(y, 1)$

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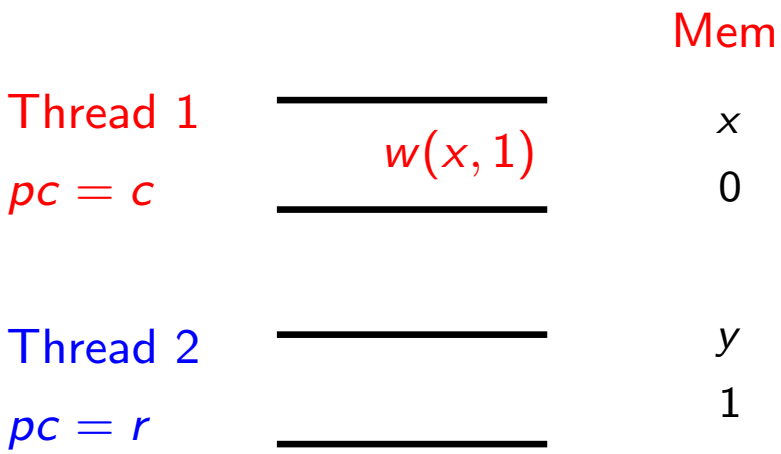

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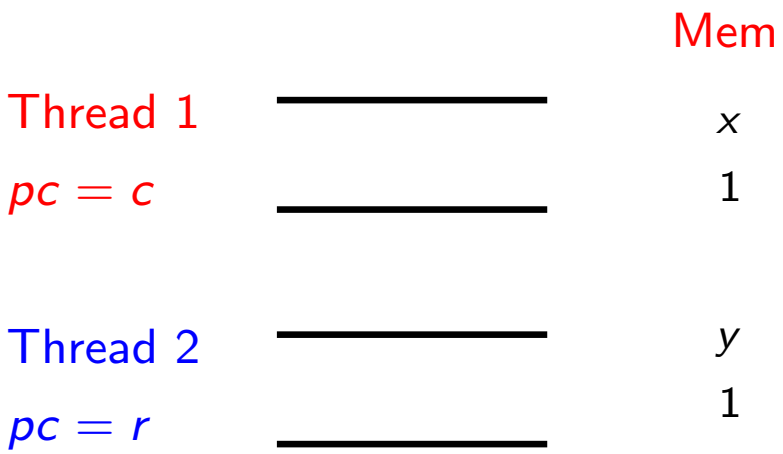

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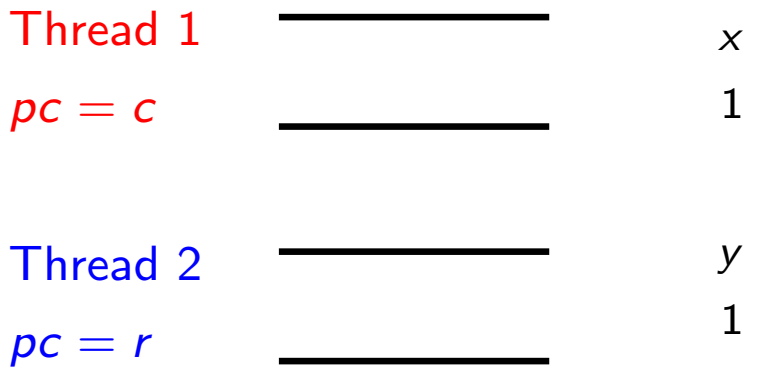

$r(y,0) \cdot w(y,1) \cdot r(x,0) \cdot w(x,1)$

Traces 2/2

Traces abstract computations to happens before dependencies

$\mathsf{Trace}(r(y,0) \cdot w(y,1) \cdot r(x,0) \cdot w(x,1))$

Traces 2/2

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- Program order: Order of actions issued by a thread

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- Conflict relation: *read* is overwritten by *write*.

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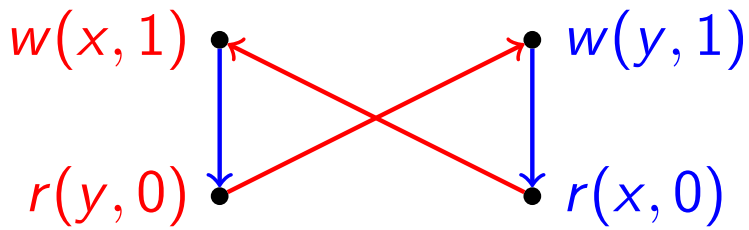

Trace Robustness Problem

Consider a memory model MM

Trace Robustness Problem against MM

Input: *Program* P.

Problem: *Does* $Traces_{MM}(P) \subseteq Traces_{SC}(P)$ *hold?*

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Proof method

Theorem [Shasha, Snir 1988]

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Shasha and Snir do not give an algorithm to find cyclic traces!

Robustness

[Bouajjani, M., Möhlmann, ICALP'11]

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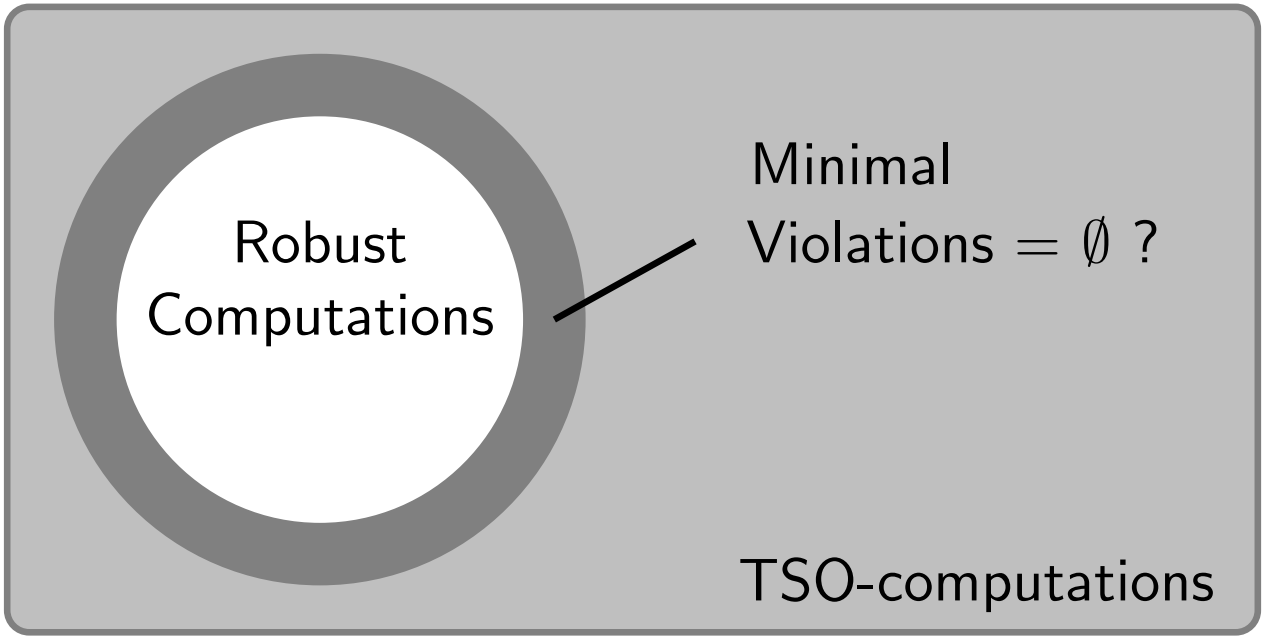
Upper Bound:

Combinatorics

From Robustness to SC Reachability

Deciding Robustness



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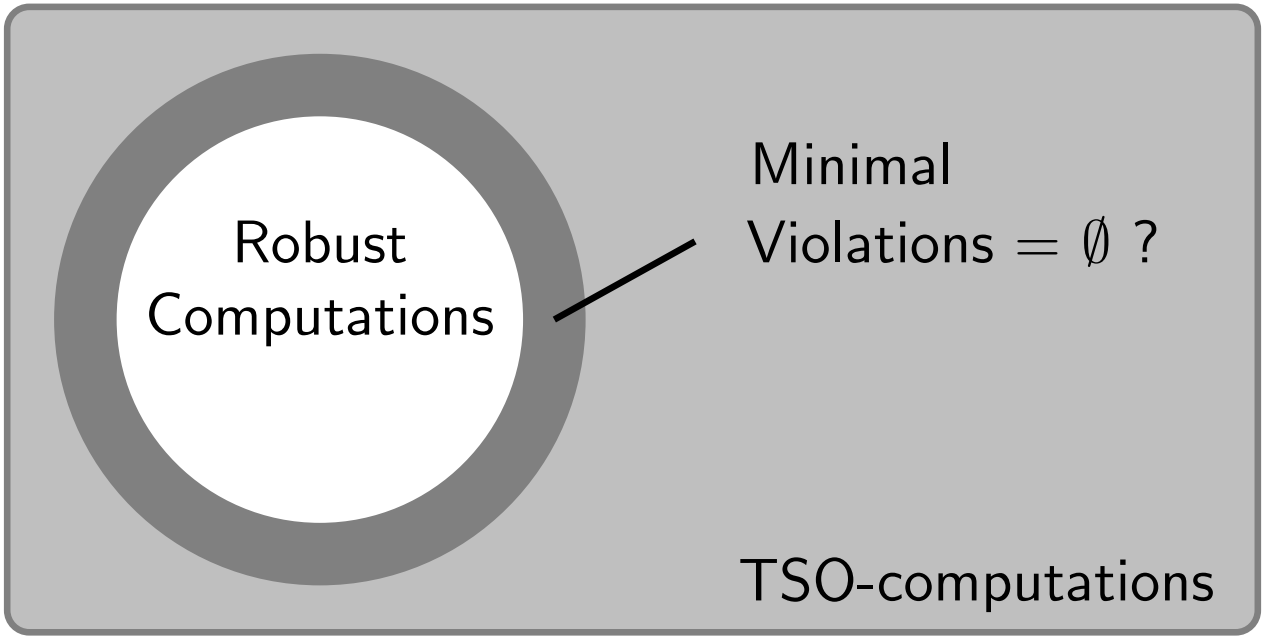

Understand shape of minimal violations

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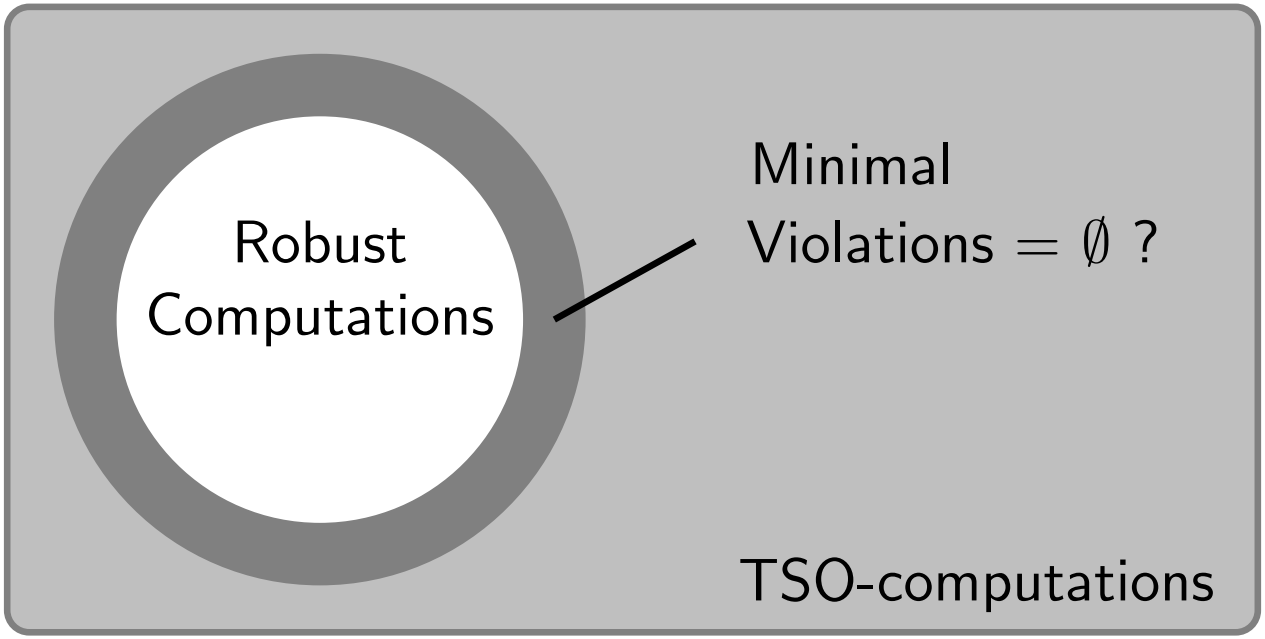

Understand shape of minimal violations

Check whether computation of this shape exists

Robustness

[Bouajjani, M., Möhlmann, ICALP'11]

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Upper Bound:

Combinatorics — Locality and Attacks

From Robustness to SC Reachability

Locality of Robustness 1/3

Goal: Locality

We can restrict ourselves to violations where only one thread reorders its actions.

Proof tool: Minimal violations

Number of inversions (out-of-program-order placements) minimal among all violating computations

Locality of Robustness 2/3

Consider minimal violation $\alpha \cdot b \cdot \beta \cdot a \cdot \gamma$ where b has overtaken a

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Subword $b_1 \dots b_k$ with

$$b_i \rightarrow_{src/st/cf} b_{i+1} \qquad \text{or} \qquad b_i \rightarrow_p^+ b_{i+1}$$

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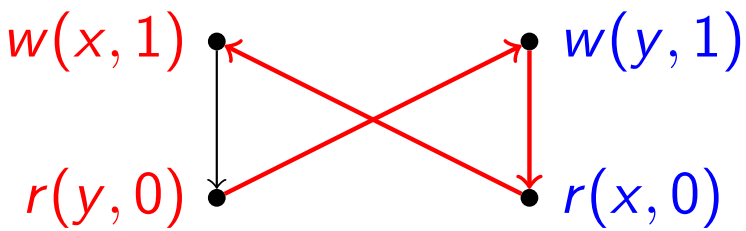

$$\underbrace{r(y,0) \cdot w(y,1) \cdot r(x,0) \cdot w(x,1)}_{\rightarrow_{hb}}$$

Locality of Robustness 3/3

Theorem (Locality) [BMM 2011]

In a minimal violation, only a single thread uses its buffer.

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Proof sketch

Pick last writes that are overtaken in two threads t_i and t_j:

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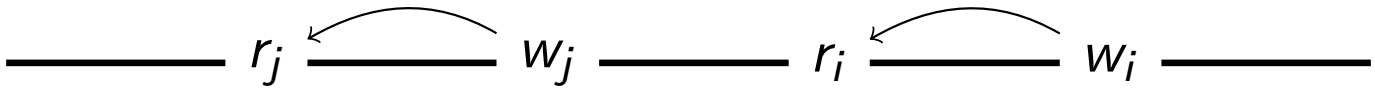

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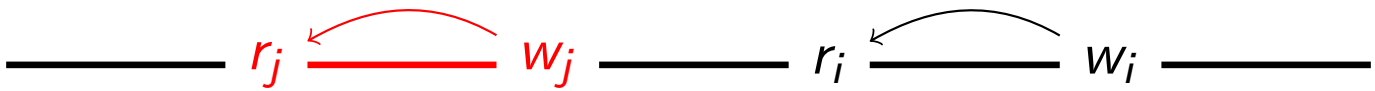

Lemma: happens before cycle $r_j \rightarrow_{hb}^{+} w_j \rightarrow_{p}^{+} r_j$

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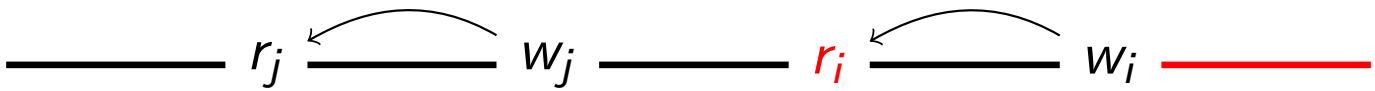

Lemma: happens before cycle $r_j \rightarrow_{hb}^{+} w_j \rightarrow_{p}^{+} r_j$
Read r_i not involved, delete everything from r_i on

Locality of Robustness 3/3

Theorem (Locality) [BMM 2011]

In a minimal violation, only a single thread uses its buffer.

Proof sketch

Pick last writes that are overtaken in two threads t_i and t_j:
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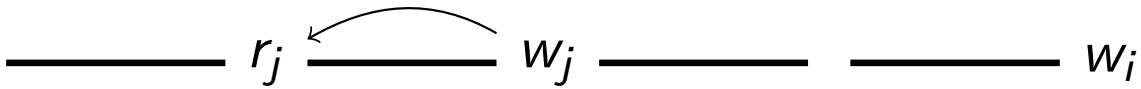

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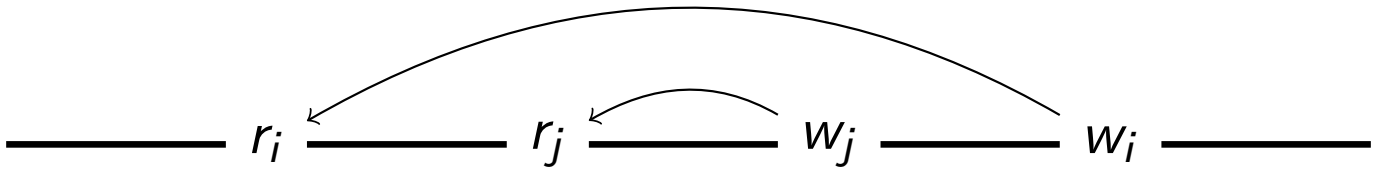

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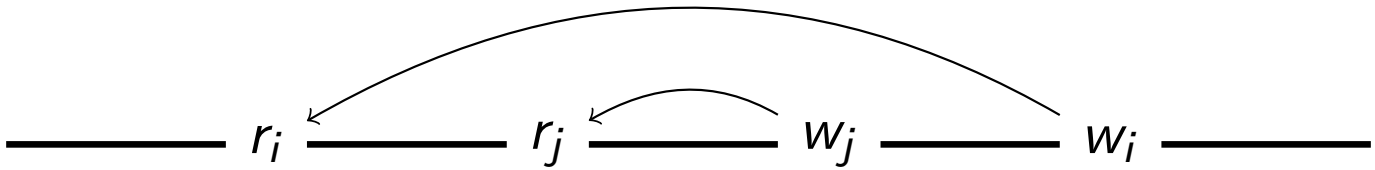

Argumentation similar, delete again r_i

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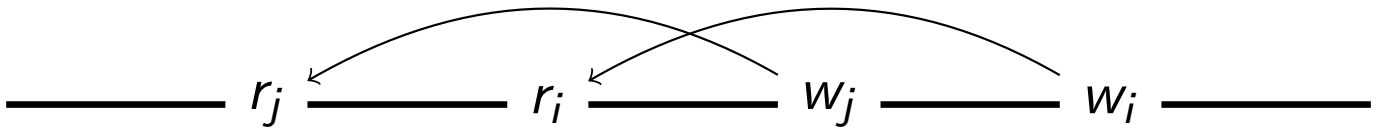

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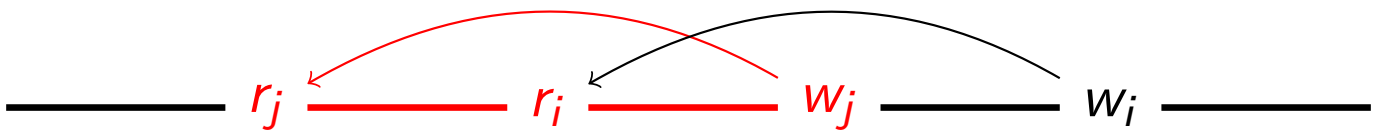

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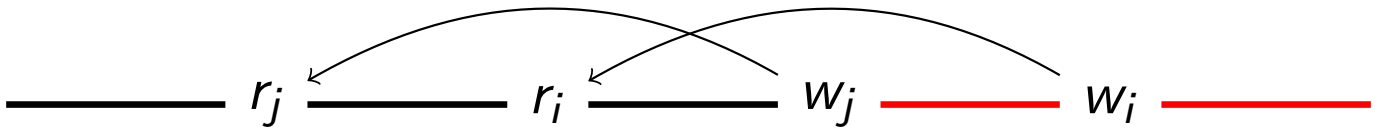

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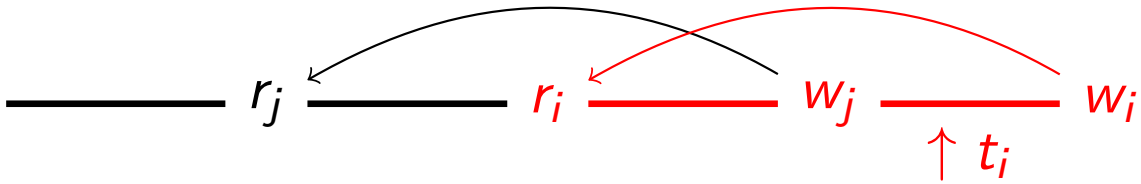

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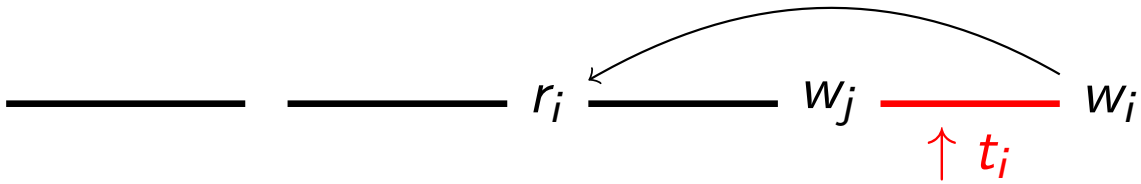

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Characterization of Robustness via Attacks 1/2

Reformulate Robustness

absence of feasible attacks

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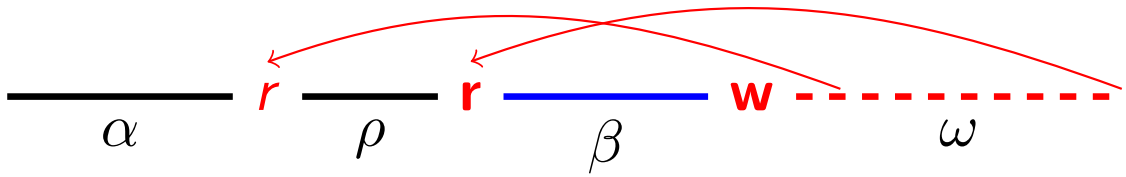

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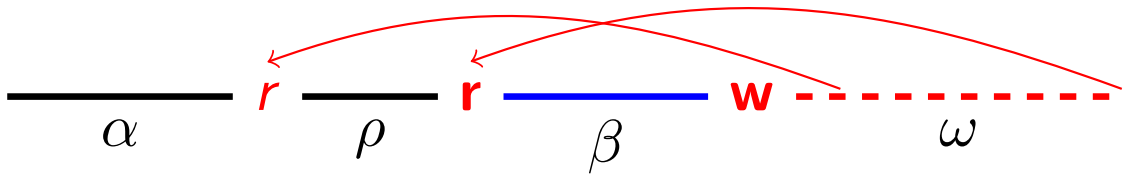

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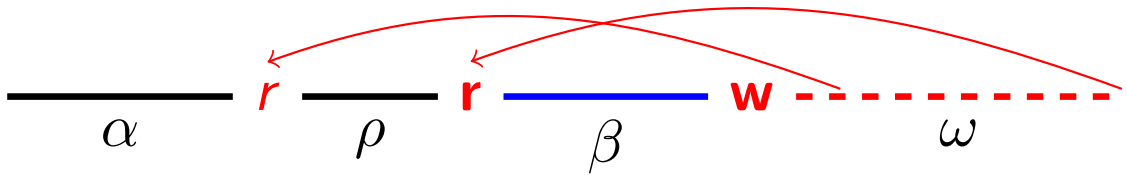

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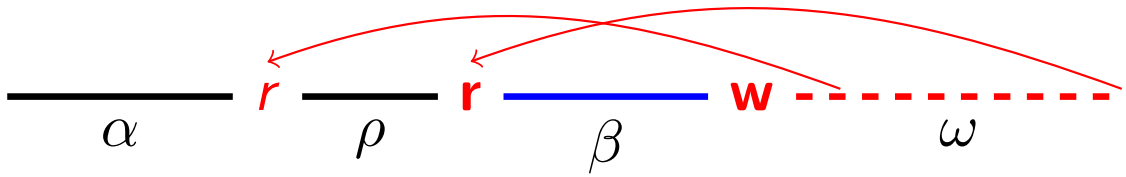

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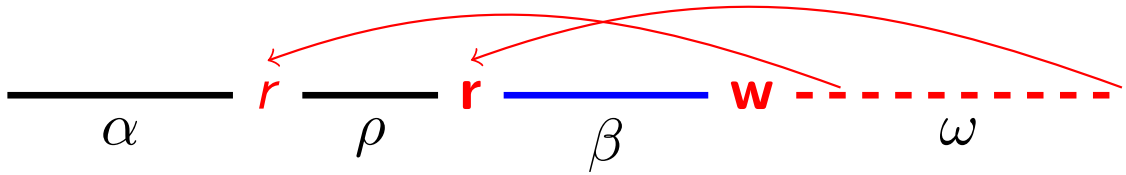

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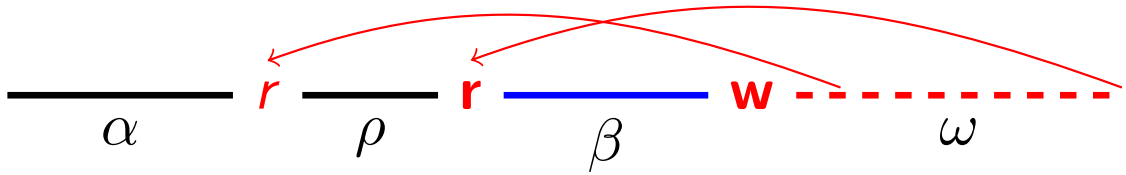

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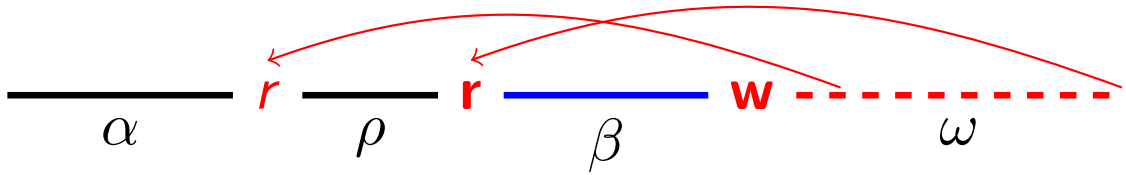

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The number of attacks is quadratic in the size of P.

Robustness

[Bouajjani, M., Möhlmann, ICALP'11]

[Bouajjani, Derevenetc, M., ESOP'13]

Upper Bound:

Combinatorics

From Robustness to SC Reachability

Finding TSO Witnesses with SC Reachability

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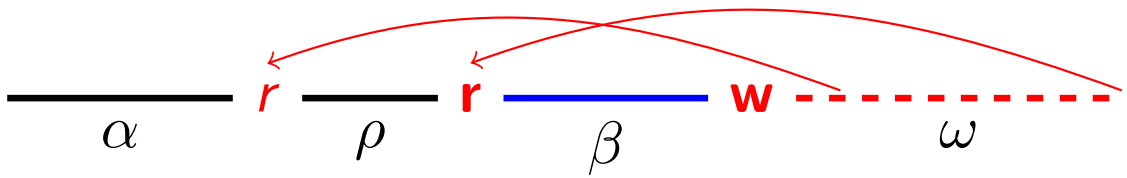

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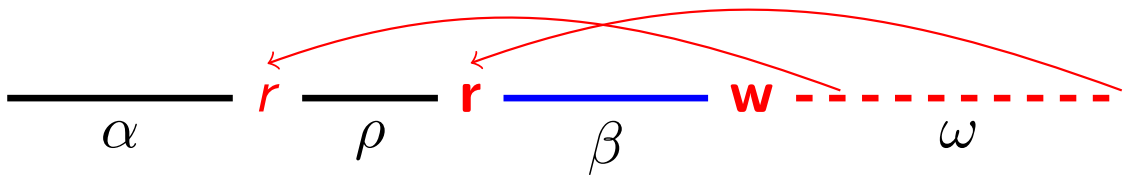

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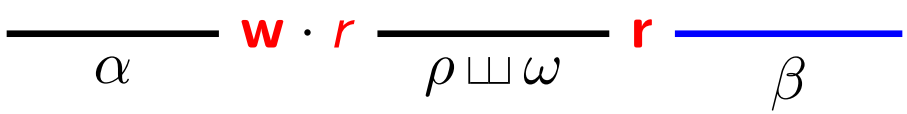

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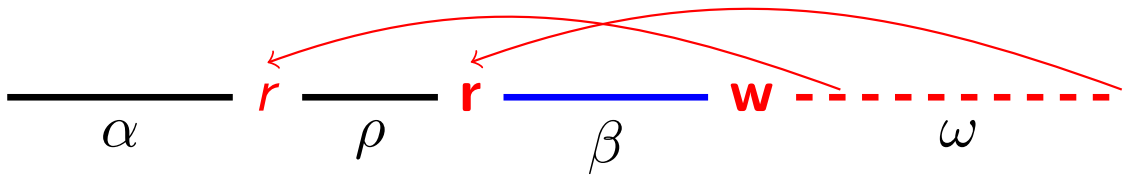

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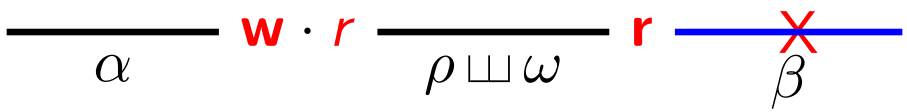

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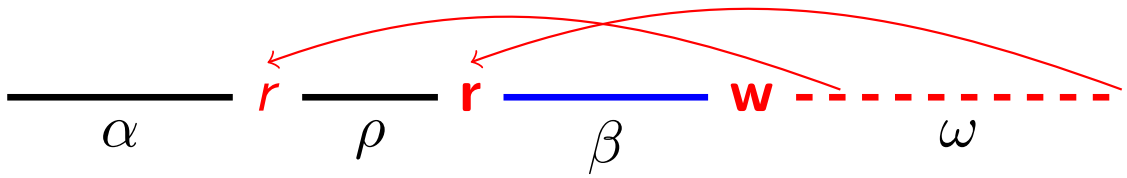

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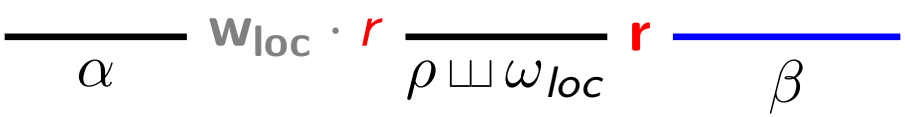

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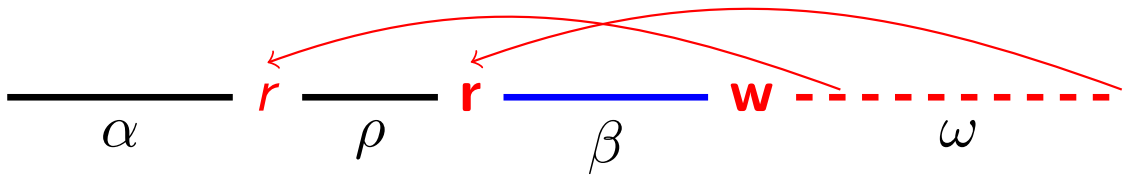

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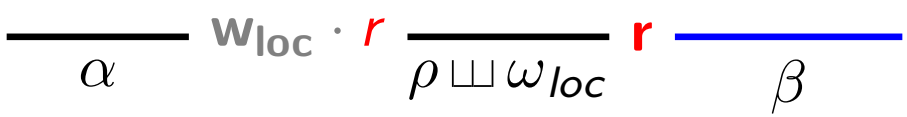

Theorem [BDM'13]

Attack A has a TSO witness iff P_A reaches goal state under SC.

Trace Robustness: Conclusion

- Decidable for TSO (and beyond)
- Is an easy problem — PSPACE-complete
- Locality: only one thread uses the buffer
- Analysis parallelizable
- Monitoring techniques:

  e.g., [Burckhardt, Musuvathi CAV'08, Sen et al. TACAS'11]

- Static analysis:

  [Shasha Snir TOPLAS'88, Alglave, Maranget CAV'11]

- Semantics:

  [Owens ECOOP'10]